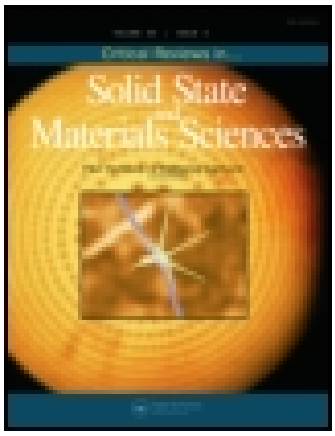

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Electrical Modeling of Thin-Film Transistors

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Electrical Modeling of Thin-Film Transistors

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An overview of device physics-oriented electrical modeling of thin-film transistors (TFTs) is presented. Four specific models are considered: (i) square-law, (ii) 3-layer, (iii) comprehensive depletion-mode, and (iv) discrete trap. For each model, a functional assessment of model equations is undertaken in terms of independent and dependent variables, model parameters, physical operating parameters, and constraining inequalities in order to facilitate mapping of model equations into a corresponding equivalent circuit. Channel mobility and "subthreshold" current trends are elucidated. Finally, a conductance integral equation based on Shockley's gradual channel approximation is introduced and is employed in model development and device assessment.

Keywords thin-film transistor, device modeling, square-law model, 3-layer model, comprehensive depletion-mode model, discrete trap model, conductance integral equation, channel mobility, fringing current artifacts, series resistance, trapping

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I. INTRODUCTION

Literature devoted to device physics assessment of thin-film transistor (TFT) operation can be categorized into three eras, the 1960s,[1–3] the 1980s,[4–6] or relatively recent.[7–12] These diverse dates reflect, respectively, the birth of TFTs, the realization of amorphous silicon TFTs for display applications, and the development of polycrystalline silicon TFTs for display and other applications, as well as a resurgent interest in TFTs for emerging applications involving large-area, low-cost, printed, flexible, and/or transparent electronics.

There are several possible reasons for undertaking electrical device modeling. Probably the most common device modeling objective is to develop circuit-oriented SPICE models in order to facilitate computer-aided design of circuits and electronic systems. Other objectives include understanding the physical nature of device operation and device optimization. Several excellent references dedicated to modeling have recently been published.[11–12] These references focus specifically on amorphous and polycrystalline silicon TFT modeling, concentrating on materials topics pertinent to such devices including band-tail and localized gap states, dispersive transport, threshold voltage metastability, diffusion current, as well as grain boundary trapping, passivation, and transport. The present article does not concern these topics as they are more pertinent to fully developed material systems and, in some cases, for example, diffusion current, are not applicable to the wide-bandgap materials of primary interest to this article.

Rather, the objective of this review article is to present an overview of generic device modeling of electrical properties of a TFT from the perspective of the development of new materials and emerging applications. Our motivation for pursuit of this topic stems from our recent research efforts in the development of transparent electronics. It is our experience that the type of modeling presented herein is useful for the elucidation of nonideal device characteristics, which are often encountered in the development of new TFT materials and device structures.[13–18] Thus, it is our hope that the models discussed herein will find use in the advancement of organic, oxide-based, or other types of emerging or future TFT technologies.

This article is not a "review article" in the conventional sense because much of what is included has never before been published. Moreover, even when classical topics are addressed, we have attempted to present them from a unique perspective.

The topics included in this article are as follows. Background information, including basic device structure and operation, an overview of the ideal square-law model, and typical nonidealities encountered in wide band gap TFTs are discussed in section II. A more complete discussion of the ideal square-law model, including series resistance effects, is given in section III. Section IV models the effects of a conductive channel. Section V is devoted to a discrete trap model, which is useful for elucidating many types of TFT device electrical characteristic trends, because traps almost always play a fundamental role in TFT operation. Additionally, the effects of the discrete trap in establishing both subthreshold and above-threshold regimes of operation are discussed. Channel mobility is considered in section VI. Two types of mobility, average and incremental mobility, are proposed as preferable replacements for the more venerable effective and field-effect mobilities typically utilized in field-effect transistor (FET) assessment. Simulations employing the discrete trap model demonstrate the importance of trapping in establishing mobility trends. Finally, the Appendix provides a derivation of the ideal square-law model equations and discusses the effects of series resistance, which do not significantly affect

the prototypical staggered bottom-gate, wide band gap TFTs, but may be useful for TFTs based on other channel materials and structures. Additionally, the conductance integral equation is introduced and is applied to derive current-voltage equations for both an enhancement-mode and a depletion-mode TFT. Finally, the discrete trap model equations are also derived in the Appendix.

II. BACKGROUND

The primary objective of this section is to provide a general background of thin-film transistors. First, several TFT device structures and fundamental device operation are discussed. Second, quantitative analysis of an ideal TFT is provided. Finally, several non-idealities observed in the development of wide band gap channel materials are discussed. However, note that non-idealities specific to circuit design or implementation, such as parasitic resistances, parasitic capacitances, and short-channel effects are not considered.

A. Device Structure and Operation

Four possible TFT device structures are shown in Figure 2.1.[10] Devices can be either staggered or coplanar. In a coplanar configuration, as shown in Figures 2.1(b) and 2.1(d), the source/drain contacts and the insulator are on the same side of the channel. In such an arrangement, the source/drain contacts are in direct contact with the induced channel such that current flows in a single plane. In a staggered configuration, as shown in Figures 2.1(a) and 2.1(c), the source/drain contacts are on the opposite side of the channel from the insulator. Thus, there is no direct connection to the induced channel. Current must flow vertically to the induced channel before flowing horizontally toward the drain. However, the contact area is very large when a staggered structure is used, resulting in minimal contact resistance.

In addition to coplanar and staggered configurations, TFTs can be classified as either bottom-gate or top-gate devices. In a bottom-gate TFT, which is sometimes referred to as an inverted TFT, the gate insulator and gate electrode are located beneath the channel, as shown in Figures 2.1(a) and 2.1(b). The top surface of a bottom-gate TFT is exposed to air or passivated by coating the top surface with a protective layer. A top-gate TFT, as shown in Figures 2.1(c) and 2.1(d), has the gate and insulator located on top of the channel. In a top-gate device, the channel is covered by a gate insulator so that the top surface is inherently passivated.

Figure 2.2 shows several ideal energy band diagrams (neglecting any passivation layer) as viewed through the gate of

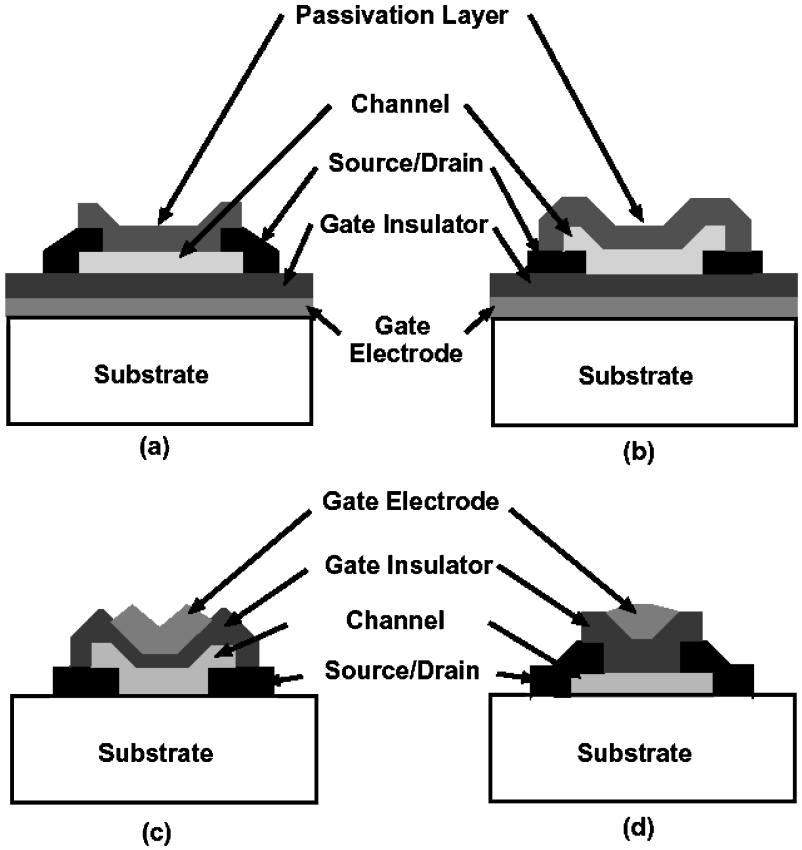

FIG. 2.1. Four general thin-film transistor configurations, including: (a) staggered bottom-gate, (b) coplanar bottom-gate, (c) staggered top-gate, and (d) coplanar top-gate.

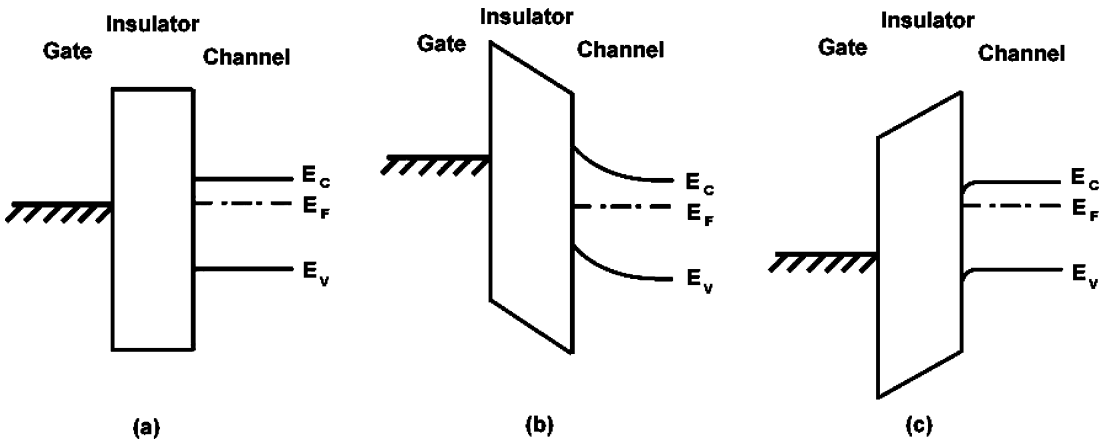

FIG. 2.2. Energy band diagrams as viewed through the gate for several biasing conditions: (a) equilibrium, (b) depletion ($V_{GS} <$ 0 V), and (c) accumulation ($V_{GS} > 0$ V).

an n-channel, accumulation-mode TFT.[3] The energy band diagram of Figure 2.2(a) shows the device at equilibrium, that is, 0 V applied to the source, drain, and gate. Figure 2.2(b) shows an energy band diagram with the gate negatively biased. The applied negative bias repels mobile electrons from the channel, leaving a depletion region near the channel/insulator interface. When compared to Figure 2.2(a), this biasing condition has reduced conductance due to a reduced number of mobile electrons in the channel. Figure 2.2(c) shows an energy band diagram with the gate positively biased. The applied positive bias attracts mobile electrons, forming an accumulation region near the insulator–channel interface. These excess mobile electrons lead to an increase in the conductance.

Beginning with the case shown in Figure 2.2(c), consider the effect of an applied drain to source voltage, V_{DS}. As V_{DS} is increased from 0 V, the channel is initially modeled as a resistor, that is, current increases linearly with increasing V_{DS}. However, as V_{DS} increases, accumulation near the drain decreases. As V_{DS} is increased further, the region near the drain eventually begins to deplete. The voltage at which the channel region near the drain is fully depleted of electrons, or pinched off, is denoted the saturation voltage, V_{DSAT}. Therefore, application of $V_{DS} \geq V_{DSAT}$ results in a saturated drain current characteristic.

A distinguishing feature of a TFT compared to a conventional metal-oxide-semiconductor field-effect transistor (MOSFET) is that carrier transport in the channel typically occurs in an *accumulation* layer in a TFT and in an *inversion* layer in a MOSFET. A TFT, just like a MOSFET, can operate as either an *enhancement*-mode or a *depletion*-mode device. Enhancement-mode devices are *normally off*, that is, negligible drain current flows at zero gate bias. Such normally off devices dissipate less power when in a standby mode, and also more readily facilitate the accomplishment of digital logic and analog circuit functions. This is in contrast to depletion-mode devices, which are *normally on* devices; such devices are useful for certain electronic applications, for example, active-load for a logic inverter, but, in general, are not as valuable electronic components for designing circuits and systems.

B. Ideal Square-Law Model Overview

As discussed in the previous subsection, the current that flows in a TFT is dependent on two applied voltages, V_{GS} and V_{DS}. For an ideal transistor, the drain current is described by the square-law model equations.[2,19] For drain voltages less than V_{DSAT}, the ideal square-law model states that

$$I_D = \frac{Z\mu C_G}{L}\left[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}\right], \quad (V_{DS} < V_{DSAT}) \qquad [2.1]$$

where I_D is the drain current, Z is the channel width, L is the channel length, μ is the mobility, V_{ON} is the turn-on voltage, and C_G is the gate capacitance per unit area. When V_{DS} greater than $V_{GS} - V_{ON}$ is applied, the channel is pinched off and the drain current is saturates at

$$I_{DSAT} = \frac{Z\mu C_G}{2L}(V_{GS} - V_{ON})^2 .(V_{DS} \geq V_{DSAT}) \qquad [2.2]$$

A complete derivation of the ideal-square law model is presented in section III.A, and also in section X.B in the context of the conductance integral equation.

Equations 2.1–2.2 are the central equations constituting the square-law model. The "square-law" designation arises from the quadratic dependence displayed in Eq. 2.2 in which the saturation current is proportional to the square of the applied gate voltage in excess of the turn-on voltage. Those familiar with the ideal square-law may notice that the threshold voltage, V_T, has been replaced by V_{ON} in Eqs. 2.1 and 2.2. In this article, V_T and V_{ON} are utilized as follows. V_T is the extrapolated value from the linear portion of a pre-pinch-off $I_D - V_{GS}$ curve, thus giving the voltage at which appreciable current flows. V_{ON} quantifies the onset of drain current conduction through the use of

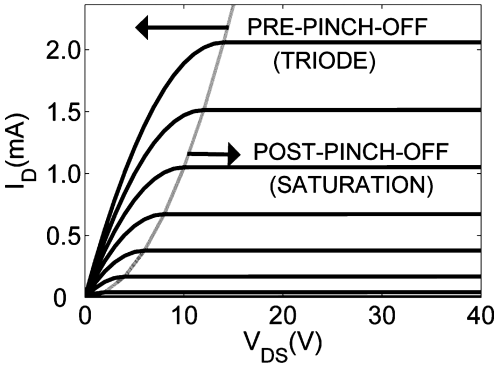

FIG. 2.3. Simulated drain current-drain voltage ($I_D - V_{DS}$) characteristics for an n-channel, depletion-mode TFT modeled using the ideal square-law model. The dashed curve identifies a locus of V_{DSAT}'s. The top curve corresponds to a gate voltage of 9 V, with the gate voltage decremented by 2 V for each subsequent curve. Square-law model parameters employed for this simulation are: $V_{ON} = -5$ V, $C_G = 70$ nF/cm^2, $\mu = 30$ cm^2/V-s, and $Z/L = 10{:}1$.

the $\log(I_D) - V_{GS}$ characteristic. A more detailed discussion of these quantities is provided in section V.B.

Several assumptions are made in the derivation of the square-law model. The primary assumption is the gradual channel approximation. The gradual channel approximation assumes that in the channel, the electric field perpendicular to the channel is much greater than the electric field parallel to the channel. This assumption allows the two electric fields to be considered separately. The second major assumption is that charge in the channel varies linearly with respect to applied gate bias. Finally, it is assumed that all induced charge is due to free carriers, which have a uniform mobility.

The most fundamental attribute of a TFT is its set of $I_D - V_{DS}$ characteristics. Figure 2.3 illustrates $I_D - V_{DS}$ behavior for varying values of V_{GS} simulated using the ideal square-law model. Several aspects of these characteristics merit consideration.

First, this TFT operates in depletion-mode, as evident from the fact that an appreciable current flows (sixth curve from the top) even when no gate voltage is applied. Enhancement-mode operation, in which negligible current flows until a sufficiently large positive voltage is applied to the gate (i.e., $V_{ON} > 0$ V), is preferable to depletion-mode behavior because circuit design is easier and power dissipation is minimized when normally off, enhancement-mode devices are employed.

Second, each $I_D - V_{DS}$ curve is comprised of a pre-pinch-off or triode regime, described by Eq. 2.1, and a post-pinch-off or saturation regime at which the current is constant with respect to V_{DS} and is given by Eq. 2.2. These two operating regimes intersect at $V_{DS} = V_{DSAT} = V_{GS} - V_{ON}$, which corresponds to the minimum drain voltage at which the entire channel thickness near the drain is depleted of free carriers.

Third, the ideal device shown in Figure 2.3 exhibits "hard saturation," as witnessed by the fact that the slope of each I_D curve is zero in the post-pinch-off or saturation regime. Hard saturation indicates that the entire thickness of the channel is depleted of free carriers. Hard saturation is desirable for most circuit applications, because a transistor exhibiting this property possesses large output impedance.

A fourth and final aspect of Figure 2.2 that warrants comment involves the magnitude of the current. A large I_D is always desirable. An assessment of Eq. 2.2 indicates that there are three primary ways to increase I_D. First, modifying the TFT geometry by increasing the magnitude of Z/L increases I_D. Second, increasing the gate dielectric constant, and hence the gate capacitance, C_G, results in more current. Finally, a higher mobility yields higher current.

C. Model Non-Idealities

Several non-idealities must be considered in order to accurately model the current-voltage characteristics of a wide band gap TFT.

First, it is possible that series resistance at the source and/or the drain can lead to a decrease in the drain current and to a concomitant apparent decrease in the channel mobility. In practice, we usually find series resistance to be of negligible importance in determining the operation of a wide band gap TFT. However, for completeness, series resistance effects related to the drain current and to the mobility are considered in sections III.C and VI.D, respectively.

Second, if a high "bulk" carrier concentration is present in the channel of a TFT, the induced charge density does not vary linearly with respect to the applied gate voltage, as assumed in the ideal square-law model. This conductive channel case is treated in section IV in terms of the 3-layer model and, more accurately, the comprehensive depletion-mode model. The comprehensive depletion-mode model is developed in the context of the conductance integral equation, as described in section X.B.

Third, traps play a critical role in determining TFT operation. Trapping of carriers injected into the channel is responsible for many subthreshold and above-thresehold trends, as presented in sections V.B and V.C, respectively, in the context of the discrete trap model, as previously introduced by Sze.[3] Additionally, carrier trapping leads to mobility degradation, as discussed in section VI.E.

Fourth, many TFT current-voltage non-idealities involve the channel mobility. We contend that the use of average and incremental mobility instead of effective and field-effect mobility results in less ambiguity when trying to understand channel mobility trends. These and other mobility issues are discussed in section VI. As already mentioned, series resistance or trapping degrade the apparent or actual channel mobility, respectively, as described in sections VI.D and VI.E. Additionally, an unpatterned channel layer results in fringing current flowing around the channel edges of a TFT. This leads to possible overestimation of the channel mobility, as considered in section VI.F. Finally, surface roughness scattering can affect the mobility of carriers in the large applied gate bias regime. This effect, although not

directly considered in this article, can easily be taken into account, either as a model refinement or using empirical data, via the conductance integral equation introduced in section X.B. Moreover, the conductance integral equation can be used to develop new model equations that account for any arbitrary conductance effect.

III. SQUARE-LAW MODEL

A. Model Derivation

In 1963, Borkan and Weimer[20] published their analysis of TFT device behavior based on Shockley's gradual channel approximation analysis of the junction field-effect transistor. The essence of this gradual channel approximation is as follows. Field-effect transistors inherently pose a two-dimensional electric field problem, involving electric field components both parallel and perpendicular to the flow of current in the channel. Shockley's gradual channel approximation invokes the assumption that the lateral change in the electric field along the channel (y-component) is much less than the change in the electric field perpendicular to the channel (x-component).[21] By making this assumption, the two-dimensional electric field problem simplifies into two separate one-dimensional problems involving gate voltage modulation of carriers in the channel and drain voltage-induced transport of carriers along the channel. It is important to note that the gradual channel approximation is only valid for long-channel devices, where the lateral electrical field can be neglected, and for device operation in the pre-pinch-off regime, as defined in the following discussion.

We begin the development of the ideal square-law model by treating the TFT gate, insulator, and semiconductor channel as an ideal metal-oxide-semiconductor (MOS) capacitor and employing the relationship $Q = C \times V$ to determine the total induced charge. Substituting in appropriate terms, we obtain,

$$q\Delta n(y) = \frac{C_G}{h}\left[V_{GS} - V(y)\right], \qquad [3.1]$$

where $q\Delta n(y)$ is the gate-induced charge density, C_G is the gate capacitance per unit area, V_{GS} is the gate voltage, h is the thickness of the semiconductor channel, and $V(y)$ is the channel voltage obtained at a distance "y" along the channel.

Assuming that mobility, μ, is constant along the channel and that the channel current is dominated by drift, the drain current, I_D, is given by,

$$I_D = hZ\left[\sigma_o + \sigma(y)\right]\xi(y), \qquad [3.2]$$

where Z is the channel width, $\xi(y)$ is the electric field along the channel, σ_o is the channel conductivity at zero gate bias, and $\sigma(y)$ is the channel conductivity due to the induced charge density. The drain current may be rewritten by noting that $\sigma = q\mu n$, resulting in,

$$I_D = hZq\mu\left[n_o + \Delta n(y)\right]\xi(y), \qquad [3.3]$$

where n_o is the initial carrier density in the semiconductor and $\Delta n(y)$ is the gate-induced carrier density. Substituting Eq. 3.1 into Eq. 3.3 and expressing the electric field in terms of the voltage drop along the channel yields,

$$I_D = Z\mu C_G\left[\frac{qhn_o}{C_G} + V_{GS} - V(y)\right]\frac{dV(y)}{dy}. \qquad [3.4]$$

Operating on both sides of Eq. 3.4 by dy and then integrating over the length of the channel, L, we obtain,

$$I_D\int_0^L dy = Z\mu C_G\int_0^{V_{DS}}\left[\frac{qhn_o}{C_G} + V_{GS} - V(y)\right]dV(y). \qquad [3.5]$$

Performing the integrations specified in Eq. 3.5 and dividing by L yields,

$$I_D = \frac{Z\mu C_G}{L}\left[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}\right], \qquad [3.6]$$

where the turn-on voltage, V_{ON}, is given by,

$$V_{ON} = \frac{-qhn_o}{C_G}. \qquad [3.7]$$

It is important to note that Eq. 3.6 is only valid when $V_{GS} \geq V_{ON}$ and when the drain voltage is less than that required to pinch-off the channel, that is, when $V_{DS} \leq V_{GS} - V_{ON}$. Equation 3.6 is not applicable in either cut-off, that is, when $V_{GS} < V_{ON}$ or in saturation, that is, when $V_{DS} \geq V_{GS} - V_{ON}$. Saturation is specified to occur when the channel is pinched off, given by the condition $V_{DS} = V_{DSAT} = V_{GS} - V_{ON}$, which when substituted into Eq. 3.6 yields,

$$I_{DSAT} = \frac{ZC_G\mu}{2L}\left(V_{GS} - V_{ON}\right)^2. \qquad [3.8]$$

Equations 3.6–3.8 are the central equations constituting the square-law model. The "square-law" designation arises from the quadratic dependence displayed in Eq. 3.8 in which the saturation current is proportional to the square of the applied gate voltage in excess of the turn-on voltage.

A complete description of the square-law model is given in Table 3.1. Three regimes of TFT operation are indicated: cut-off, pre-pinch-off (typically denoted "triode"), and post-pinch-off (typically denoted "saturation"). The corresponding constraint relations correspond to the gate voltage with respect to V_{ON} and the drain voltage with respect to V_{DSAT}.

An important function of a device physics–based model, such as the square-law model specified in Table 3.1, is associated with its utility for circuit simulation. Development of a circuit simulation model requires mapping of device physics equations into an appropriate equivalent circuit. To accomplish this mapping in a systematic manner, it is useful to identify the independent and dependent model variables (IV, DV), model parameters (MP), and physical operating parameters (POP) and to then specify them in the following functional form,

$$DV(IV_1 IV_2, \ldots; MP_1, MP_2, \ldots; POP_1, POP_2), \qquad [3.9]$$

TABLE 3.1
Summary of the square-law model

Variable designation		Equation
Turn-on voltage		$V_{ON} = \frac{-qhn_o}{C_G}$
Pinch-off condition		$V_{DSAT} = V_{GS} - V_{ON}$
Regime of operation	Equation	Constraints
Cut-off	$I_D = 0$	$V_{GS} < V_{ON}$
Pre-pinch-off	$I_D = \frac{Z\mu C_G}{L}[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}]$	$V_{GS} \geq V_{ON}$ $V_{DS} \leq V_{DSAT}$
Post-pinch-off	$I_{DSAT} = \frac{Z\mu C_G}{2L}(V_{GS} - V_{ON})^2$	$V_{GS} \geq V_{ON}$ $V_{DS} > V_{DSAT}$
Model parameters	Geometrical-based	Z, L, h, C_G
	Channel-based	n_0, μ

Employing this procedure to square-law theory yields,

$$I_D\,(V_{GS}, V_{DS}; Z, L, n_0, h, C_G, \mu; none)\,. \qquad [3.10]$$

Expressing the square-law model in this functional form allows one to quickly discern the two independent variables, six model parameters, and zero explicit physical operating parameters. (It could be argued that n_0 and μ implicitly depend on temperature, at least in a real device, so that temperature should be considered to be an implicit physical operating parameter.)

Note that, in general, the number of model parameters is not unique because a model may be expressed in various forms. For example, a circuit engineer would typically combine, μ and C_G into one model parameter, thus reducing the number of model parameters. Model parameter specification is usually driven by the objective of the modeler. In the context of this review article, our primary motive is to elucidate TFT device physics operation. Therefore, we typically avoid model parameter compression since it tends to obscure the operating physics. As indicated in Table 3.1, model parameters can also be sub-categorized based on whether they involve device geometry or properties of the materials comprising the device.

In order to map a device physics-based model into an appropriate equivalent circuit, identification of independent and dependent variables in a functional format is essential. Thus, establishing $I_D\,(V_{GS}, V_{DS})$ in the square-law model facilitates identification of a nonlinear, *voltage-controlled current source* as an appropriate equivalent circuit element. Two voltages, V_{GS} and V_{DS} control I_D. I_D is, in general, nonlinear with respect to V_{GS} or V_{DS} as evident from Eqs. 3.6 and 3.8.

If a corresponding, but more complicated, device physics–based development is undertaken with respect to TFT capacitance-voltage (C-V) characteristics, it would require the incorporation of two additional nonlinear, voltage-controlled capacitors into the square-law, TFT equivalent circuit. Such an equivalent circuit is indicated in Figure 3.1. Because our primary modeling focus involves DC $I_D - V_{DS}$ and $I_D - V_{GS}$ assessment, we do not include C-V modeling in this review except with respect to specification of equivalent circuits for the models discussed herein. However, it should be recognized that inclusion of these nonlinear, voltage-controlled capacitors are required for AC or transient modeling of TFTs.

B. Simulation Results

Figure 3.2 shows simulated I_D characteristics using the ideal square-law model. In Figure 3.2(a), the $I_D - V_{DS}$ characteristic (V_{GS} is decreased from 9 to −3 V in 2 V steps) is shown. This simulation results in ∼2 mA maximum current drive. In Figure 3.2(b), $I_D - V_{GS}$ curves with $V_{DS} = 1$ V, employing channel mobilities of 10 and 30 cm^2/V-s are shown. Not only does the mobility affect the magnitude of the current at a given V_{GS} value, but it also changes the slope. Note that in the ideal case shown here, abrupt drain current turn-on at V_{ON} is observed. Moreover, for this ideal situation, V_T is equivalent to V_{ON} ∼–5 V because the effect of carrier trapping, which is considered in section V, is neglected here.

C. Series Resistance Effects

We begin our analysis of series resistance effects with the square-law model derived in the previous sub-section. Building on the square-law equivalent circuit model, resistors R_D and R_S are added at the source and the drain, as indicated in Figure 3.3.

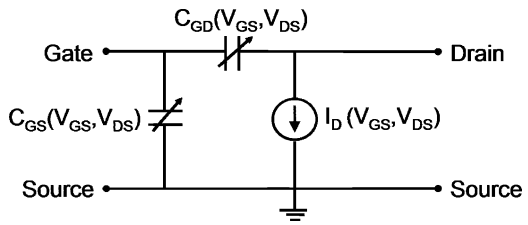

FIG. 3.1. An equivalent circuit consisting of two nonlinear, voltage-controlled capacitors and a nonlinear, voltage-controlled current source corresponding to the square-law model specified by Table 3.1.

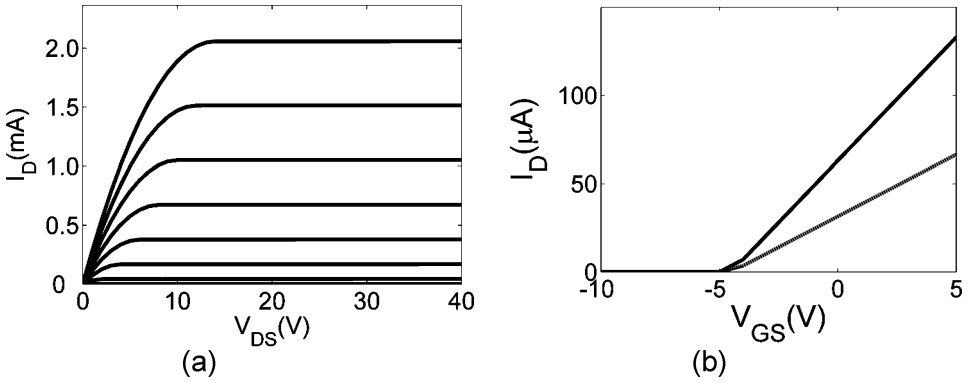

FIG. 3.2. Simulated (a) $I_D - V_{DS}$ and (b) $I_D - V_{GS}$ curve characteristics using the ideal square-law model. For the (a) $I_D - V_{DS}$ characteristic, V_{GS} is decreased from 9 to −3 V in 2 V steps. The (b) $I_D - V_{GS}$ characteristics use $V_{DS} = 1$ V and μ =10 and 30 cm^2/V-s for the grey and black curves, respectively. Square-law model parameters employed for this simulation are: $V_{ON} = -5$ V, C_G =70 nF/cm^2, Z/L = 10:1, and $\mu = 30$ cm^2/V-s (unless otherwise specified).

The addition of the series resistors results in I_D equations for the pre- and post-pinch-off regimes as follows. For the pre-pinch-off regime I_D is given by,

$$I_D = \frac{ZC_G\mu}{L}\left(V'_{GS} - V_{ON} - \frac{V'_{DS}}{2}\right)V'_{DS}$$
$$= \frac{ZC_G\mu}{L}\left(V_{GS} - I_D R_S - V_{ON} - \left(\frac{V_D - I_D(R_S + R_D)}{2}\right)\right)$$
$$\times\ (V_D - I_D\,(R_S + R_D)) \qquad [3.11]$$

where the primed quantities V_{GS}' and V_{DS}' represent internal voltages across the TFT from the gate-to-source and drain-to-source, respectively. The corresponding drain current equation for the post-pinch-off regime becomes,

$$I_D = \frac{ZC_G\mu}{2L}(V'_{GS} - V_{ON})^2$$
$$= \frac{ZC_G\mu}{2L}\,(V_{GS} - I_D R_S - V_{ON})^2 \qquad [3.12]$$

The modified pinch-off condition is given by

$$V_{DSAT} = V_{GS} - V_{ON} + I_D R_D. \qquad [3.13]$$

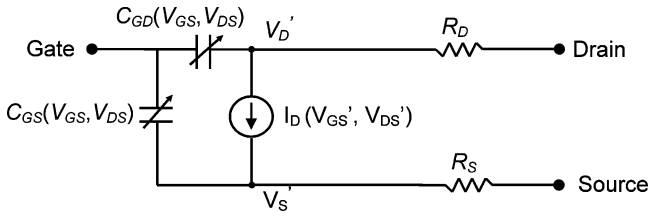

FIG. 3.3. Square-law model equivalent circuit for a TFT that includes the effects of source and drain series resistance. Primed quantities represent internal voltages.

A complete derivation of the series resistance equations, that is, Eqs. 3.11–3.13, is given in section IX.A.

A summary of the variables, equations, regimes of operation, constraints, and model parameters constituting the square-law model with the addition of series resistance is presented in Table 3.2.

It is evident from the model equations given that incorporation of R_S and R_D into the square-law model leads to a reduction in the drain current due to a concomitant decrease in effective terminal voltages. Additionally, comparing the pinch-off condition given in Eq. 3.13 reveals that V_{DSAT} has increased when compared to the ideal square-law model (excluding series resistance).

Figure 3.4 shows an example simulation which illustrates the effect of series resistance, R_{SERIES}, on an $I_D - V_{DS}$ curve. In this simulation, $R_{SERIES} = R_S + R_D$ and $R_D = R_S$. The two limits, $R_{SERIES} = 0$ (top-curve) and $R_{SERIES} = \infty\Omega$ (bottom-curve), are shown, as well as several intermediate values. At R_{SERIES} =

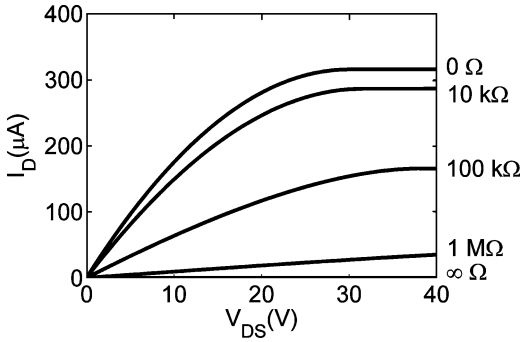

FIG. 3.4. Simulated $I_D - V_{DS}$ curves for varying values of series resistance. Parameters used for this simulation are: $V_{GS} = 30$ V, $R_{SERIES} = R_S + R_D$ and $R_S = R_D$. R_{SERIES} = [0 Ω, 10 kΩ, 100 kΩ, 1 MΩ, ∞Ω]. $Z/L = 10$, $h = 100$ nm, $C_G = 7 \times 10^{-7}$ F/cm^2, $n_0 = 10^{14}$ cm^{-3}, and $\mu = 10$ cm^2/V-s.

TABLE 3.2
Summary of the square-law model with series resistance incorporated

Variable definition		Equation
Turn-on voltage		$V_{ON} = \frac{-qhn_o}{C_G}$
Pinch-off condition		$V_{DSAT} = V_{GS} - V_{ON} + I_D R_D$
Regime of operation	Equation	Constraints
Cut-off	$I_D = 0$	$V_{GS} < V_{ON}$
Pre-pinch-off	$I_D = \frac{ZC_G\mu}{L}(V'_{GS} - V_{ON} - \frac{V'_{DS}}{2})V'_{DS}$	$V_{GS} \geq V_{ON}$ $V_{DS} \leq V_{DSAT}$
Post-pinch-off	$I_D = \frac{ZC_G\mu}{2L}(V'_{GS} - V_{ON})^2$	$V_{GS} \geq V_{ON}$ $V_{DS} > V_{DSAT}$
Model parameters	Geometrical-based	Z, L, h, C_G
	Channel-based	n_0, μ
	Series resistance-based	R_S, R_D

0, the $I_D - V_{DS}$ curve follows the ideal square-law model. As R_{SERIES} increases, an increasing fraction of the applied voltage is dropped across the parasitic series resistors, thereby internally biasing the TFT at a lower effective voltage, resulting in less current drive. Additionally, the voltage corresponding to pinch-off, which establishes the onset of saturation of an $I_D - V_{DS}$ curve, increases with increasing series resistance (e.g., $V_{DSAT} =$ 30, 30.15, 31.4, 38.3, 49.5, 57 V for $R_{SERIES} = 0$, 1 k, 10 k, 100 k, 1 M, 10 MΩ, respectively). Thus, I_D does not saturate over the domain of V_{DS} shown in Figure 3.3 when $R_{SERIES} > 1$ MΩ. The limiting case of corresponds to all of the voltage being dropped across R_D and R_S, so that V'_{GS} and V'_{DS} are zero. Thus, the $I_D - V_{DS}$ curve shows negligible current conduction when $R_{SERIES} = \infty\Omega$.

Figure 3.5 shows the effect of series resistance on an $I_D - V_{GS}$ curve using the same values for R_{SERIES} as employed for Figure 3.5. It is evident from Figure 3.5 that the slope of the $I_D - V_{GS}$ curve decreases with increasing series resistance. Note also that this slope increases nonlinearly with respect to V_{GS}.

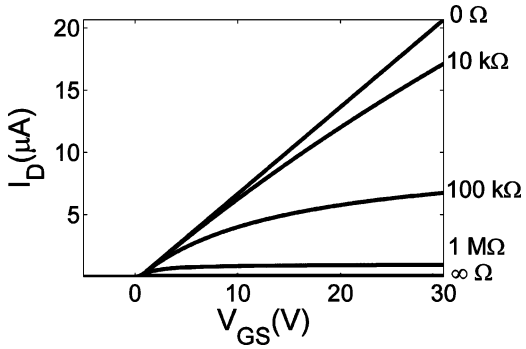

FIG. 3.5. Simulated $I_D - V_{GS}$ curves for varying values of series resistance. $R_{SERIES} = R_S + R_D$ and $R_D = R_S$. $V_{DS} = 1$ V. $R_{SERIES} = [0\ \Omega, 10\ k\Omega, 100\ k\Omega, 1\ M\Omega, \infty\Omega]$. Z/L = 10, h = 100 nm, $C_G = 7 \times 10^{-7}$ F/cm^2, $n_0 = 10^{14}$ cm^{-3}, and $\mu = 10$ cm^2/V-s.

This $I_D - V_{GS}$ trend results in a severe degradation of the apparent mobility.

As mentioned previously, we typically find series resistance to be of negligible importance in determining the operation of wide band gap, inorganic oxide TFTs, however, the analysis provided here may be useful for elucidating the effects of reduced device dimensions.

IV. CONDUCTIVE CHANNEL MODELS

The ideal square-law model presented in section III provides an excellent framework for the development of more adaptable models. In this section, the 3-layer and comprehensive depletion-mode models are introduced to account for channels with an appreciably high carrier concentration. The 3-layer model provides an extremely simple means of modeling a conductive channel by adding two additional conduction paths, in parallel with the gate-induced channel current. Due to the simplicity of the 3-layer model, however, it has several deficiencies; these deficiencies are addressed in the comprehensive depletion-mode model.

A. 3-Layer Model Overview

Figure 4.1 illustrates the 3-layer model. Two additional conduction paths are included in Figure 4.1 in addition to the "normal" drain current component, $I_{D,IND}$, which corresponds to the gate-induced current path developed in section III in the square-law model. The two additional conduction paths (bulk and surface) are modeled as resistors. Current flowing through the "bulk" portion of the channel, $I_{D,BULK}$, is associated with a uniform bulk resistance of the channel,

$$R_{BULK} = \frac{L}{q\mu N_D h Z} \qquad [4.1]$$

where N_D is the bulk carrier concentration. $I_{D,SURFACE}$ is associated with $R_{SURFACE}$ and accounts for the possibility that an accumulation layer is present at the channel surface, where "surface" is used to denote the channel interface opposite to that of the semiconductor/insulator interface. Figure 4.2 illustrates

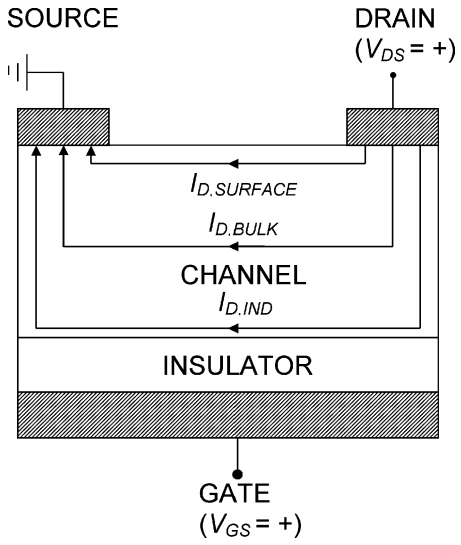

FIG. 4.1. A schematic of the 3-layer model for a simplified bottom-gate TFT with an n-type channel.

an energy band diagram showing the formation of a surface accumulation layer at zero-bias for a bottom-gate TFT with an n-type channel. The semiconductor/insulator interface is idealized in Figure 4.2, neglecting any gate-semiconductor work function difference and interface state effects.

Mapping the model parameters into an equivalent circuit, in the same way as demonstrated in section III.A, yields,

$$I_D\,(V_{GS}, V_{DS}; Z, L, n_0, h, C_G, \mu, \mu_{SURFACE}, R_{SURFACE};\ \text{none})\,, \quad [4.2]$$

where μ and $\mu_{SURFACE}$ represent the semiconductor/insulator interface and the surface mobilities respectively, and $R_{SURFACE}$ represents the resistance of the surface accumulation layer. An equivalent circuit appropriate for the 3-layer model is given in

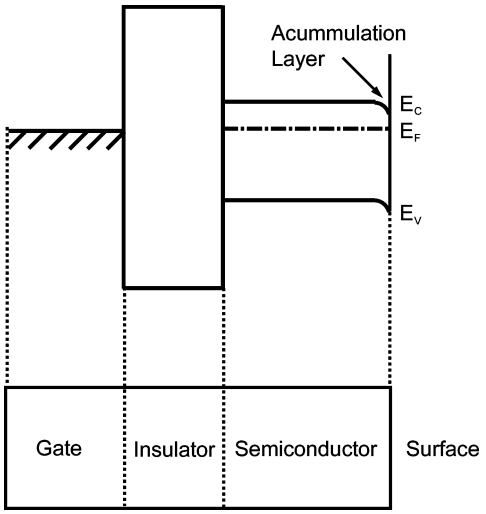

FIG. 4.2. Energy band diagram for an n-type TFT with a surface accumulation layer.

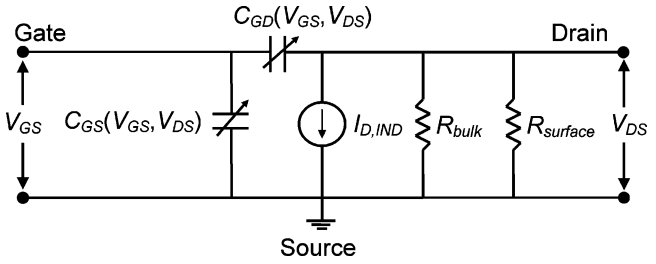

FIG. 4.3. An equivalent circuit for the 3-layer model.

Figure 4.3. Note that $I_{D,IND}$ is a voltage-controlled current source that (implicitly) depends on V_{GS} and V_{DS}.

A summary of the variables, equations, regimes of operation, constraints, and model parameters constituting the 3-layer model is presented in Table 4.1. Only two additional parameters, $\mu_{SURFACE}$ and $R_{SURFACE}$, are required to specify the 3-layer model in addition to those employed in the square-law model.

B. Application of the 3-Layer Model Applied to SnO_2 Transparent Thin-Film Transistors

With the addition of R_{BULK} into the square-law model, a large initial carrier concentration can have a dramatic effect on $I_D - V_{DS}$ curves, as shown in Figure 4.4. Figure 4.4(a)–(d) show the effect of different values of N_D, and therefore R_{BULK}, on the $I_D - V_{DS}$ curves. The simulation shown in Figure 4.4(a), with a carrier concentration of 10^{20} cm^{-3}, essentially behaves as a simple linear resistor with a bulk resistance of 2.5 kΩ. Consequently, nearly all of the current in this device flows through the bulk, resulting in linear $I_D - V_{DS}$ curves with negligible gate voltage modulation. Figure 4.4(b) displays a very small amount of gate voltage modulation in the $I_D - V_{DS}$ curves, whereas Figure 4.4(c) is beginning to behave similar to an ideal transistor. Thus, as N_D decreases, the percentage of the drain current that is attributed to gate-induced current ($I_{D,IND}$) increases, resulting in more effective gate modulation in the $I_D - V_{DS}$ curves. However, "hard" saturation of the $I_D - V_{DS}$ curves is not obtained in any case, including Figure 4.4(d). The lack of "hard" saturation is in contradistinction to characteristics exhibited by real TFTs. This is a limitation of the 3-level model. By modeling the bulk and surface conduction paths as resistors, it is implicitly assumed that these conduction paths cannot be affected by the applied gate voltage. Moreover, it is implicitly assumed that the channel cannot be fully depleted. For real TFTs with V_{ON} as low as ∼–10 V, drain current saturation is observed provided that the drain voltage is sufficiently large to obtain pinch-off.

Figure 4.5 shows measured $I_D - V_{DS}$ characteristics for a SnO_2 TTFT with a simulated fit using the 3-layer model. The high initial carrier concentration results in non-saturating characteristics for the applied voltage range, as evident from Figure 4.5. Notice that the 3-layer model provides a reasonable fit to the measured data at high gate voltages. As V_{GS} is decreased and approaches V_{ON} (which is calculated to be ∼–17 V), the

TABLE 4.1
Summary of the 3-layer model

Variable designation		Equation
Turn-on voltage		$V_{ON} = \frac{-qhN_D}{C_G}$
Pinch-off condition		$V_{DSAT} = V_{GS} - V_{ON}$
Bulk Resistance		$R_{BULK} = \frac{L}{q\mu N_D hZ}$
Regime of operation	Equation	Constraints
Cut-off	$I_D = \frac{V_{DS}}{R_{BULK}} + \frac{V_{DS}}{R_{SURFACE}}$	$V_{GS} < V_{ON}$
Pre-pinch-off	$I_D = \frac{Z\mu C_G}{L}[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}] + \frac{V_{DS}}{R_{BULK}} + \frac{V_{DS}}{R_{SURFACE}}$	$V_{GS} \geq V_{ON}$ $V_{DS} \leq V_{DSAT}$
Post-pinch-off	$I_D = \frac{Z\mu C_G}{L}(V_{GS} - V_{ON})^2 + \frac{V_{DS}}{R_{BULK}} + \frac{V_{DS}}{R_{SURFACE}}$	$V_{GS} \geq V_{ON}$ $V_{DS} > V_{DSAT}$
Model parameters	Geometrical-based	Z, L, h, C_G
	Channel-based	n_0,μ
	Surface-based	$\mu_{SURFACE}$, $R_{SURFACE}$

3-layer model fit deteriorates. This deterioration is due to the fact that the 3-layer model assumes that the channel cannot be fully depleted. Therefore, the 3-layer model should be limited to qualitative (rather than quantitative) modeling to elucidate basic device operation. To alleviate the deficiencies of the 3-layer model, depletion near the drain must be accounted for, as accomplished in the comprehensive depletion-mode model, which is introduced in the next sub-section.

C. Comprehensive Depletion-Mode Model

The comprehensive depletion-mode model presented in this sub-section addresses the deficiencies of the 3-layer model. A full derivation[22–24] of the comprehensive depletion-mode model is presented in section X.B.

Consider the nature of operation of an n-channel, depletion-mode TFT. When a positive gate voltage is applied, an accumulation layer forms at the insulator/semiconductor interface. When

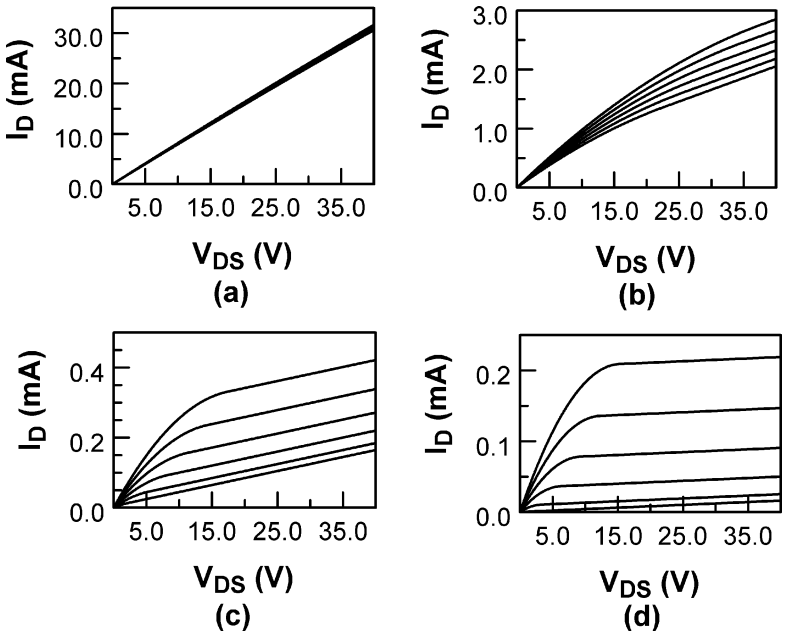

FIG. 4.4. Simulated $I_D - V_{DS}$ curves for varying values of the channel carrier concentration n_0. Plots (a)–(d) represent varying carrier concentrations of 10^{20}, 10^{19}, 10^{18}, 10^{17} cm^{-3} and result in V_{ON} ~–230, −23, −2.3, −0.2 V, respectively. Model parameters used in this simulation: $Z/L = 5$, $h = 100$ nm, $C_G = 7 \times 10^{-7}$ F/cm^2, $\mu = 0.5$ cm^2/V-s, $R_{SURFACE} = 10^9\Omega$.

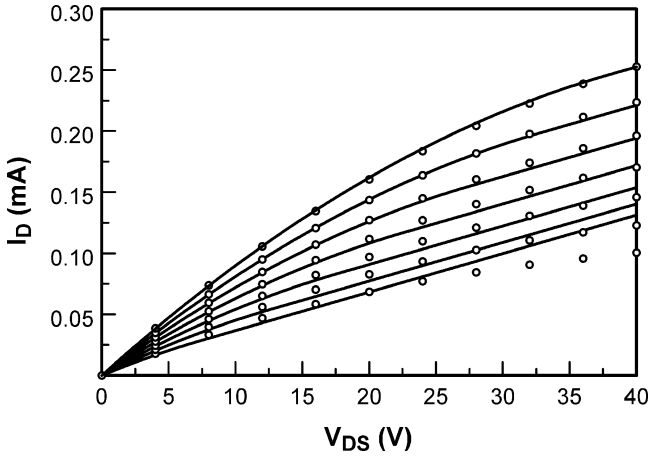

FIG. 4.5. Measured $I_D - V_{DS}$ curves (open circles) for a SnO_2 TTFT with a fit to the data (continuous lines) using the 3-layer model. V_{GS} is decreased from 20 V (top curve, showing maximum current) to −10 V in 5 V increments. Model parameters used in this simulation: $N_D = 1.3 \times 10^{18}$ cm^{-3}, $Z/L = 5$, $h = 60$ nm, $C_G = 7 \times 10^{-8}$ F/cm^2, $\mu = 0.5$ cm^2/V-s, and $R_{SURFACE} = 10^9 \Omega$.

a negative bias is applied to the gate, the interface is in depletion, but it is still possible for current to flow. When $V_G < V_{ON}$, no current flows. The regions of operation just described are summarized in the channel conductance-gate voltage ($G_D^{LIN} - V_G$) characteristic shown in Figure 4.6, where G_D^{LIN} designates that the channel conductance is evaluated in the linear region ($V_{DS} \rightarrow 0$ V).

Two transitions are evident from the dashed lines in Figure 4.6. The first transition, from the zero region to the depletion region, is established by the turn-on voltage, V_{ON},

$$V_G \left(G_D^{LIN}\big|_{DEPL} = 0 \right) \equiv V_{ON} = V_P - \frac{qN_D h}{C_G}. \qquad [4.3]$$

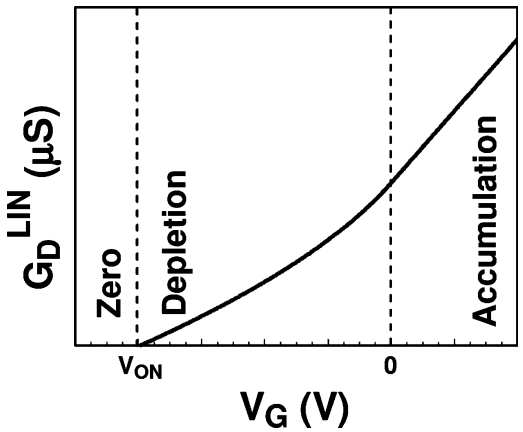

FIG. 4.6. $G_D^{LIN} - V_G$ plot for an idealized depletion-mode TFT.

Notice that the first term on the right side of Eq. 4.3 represents the pinch-off voltage, V_P, which is the voltage dropped across the semiconductor when the channel is fully depleted. V_P is given by

$$V_P = -\frac{qN_D h^2}{2\varepsilon_S}, \qquad [4.4]$$

where ε_S is the semiconductor permittivity. The second term in Eq. 4.3 is the voltage dropped across the insulator when the channel is fully depleted. Because V_P is a negative quantity, V_{ON} is thus, always a negative quantity, which is consistent with a depletion-mode TFT. The second transition, from depletion to accumulation, occurs at 0 V, assuming no semiconductor-metal work function difference or flat-band voltage shift.

Now, consider several biasing schemes, indicated by the solid lines in the $G_D^{LIN} - V_G$ plots shown in Figure 4.7. Note that the dashed lines separate the regions of operation (i.e., zero, depletion, and accumulation). Additionally, the corresponding TFT cross-sections are given to illustrate the nature of conduction. Figure 4.7(a) shows the device with applied voltages ($V_{ON} < V_{GS} < 0$ V and $V_{ON} < V_{GD} < 0$ V) such that a depletion region exists in the channel from the source to drain. Figure 4.7(b) shows the device with applied voltages ($V_{GS} > 0$ V and $V_{GD} > 0$ V) such that an accumulation region exists in the channel from the source to the drain. Figure 4.7(c) shows the intermediate case ($V_{GS} > 0$ V and $V_{ON} < V_{GD} \leq 0$ V) in which the channel is partially depleted and partially accumulated.

First, consider the depleted channel case indicated in Figure 4.7(a). A depletion region exists in the channel from the source to the drain, when both V_{GD} and V_{GS} are between V_{ON} and zero volts. Next, consider the accumulated-channel case shown in Figure 4.7(b). The channel near the source is accumulated when $V_{GS} > 0$ V and the channel near the drain is accumulated when $V_{GD} > 0$ V. In this case, the depletion-mode model accounts for the appreciable bulk carrier concentration by the addition of a resistor in parallel with $I_{D,IND}$. If the drain voltage is increased, such that V_{GD} decreases below 0 V, the channel near the drain is partially depleted, resulting in the situation shown in Figure 4.7(c). Because both an accumulation region and a depletion region exist along the length of the channel, both regions must be accounted for when calculating the channel conductance. Thus, the cases illustrated in Figure 4.7(a)–(c) correspond to the depletion (DEPL), accumulation (ACC), and accumulation-depletion (ACC-DEPL) regimes of TFT operation, respectively. The $I_D - V_{DS}$ characteristics for these regimes, as well as, the depletion-saturation (DEPL-SAT) and accumulation-saturation (ACC-SAT) regimes are shown and identified in Figure 4.8.

Table 4.2(a) and (b) summarize the variables, definitions, and central equations constituting the comprehensive depletion-mode model. Additionally, the governing V_{DS} and V_{GS} constraint relationships for each operating regime and the model parameters are given in Table 4.2(b).

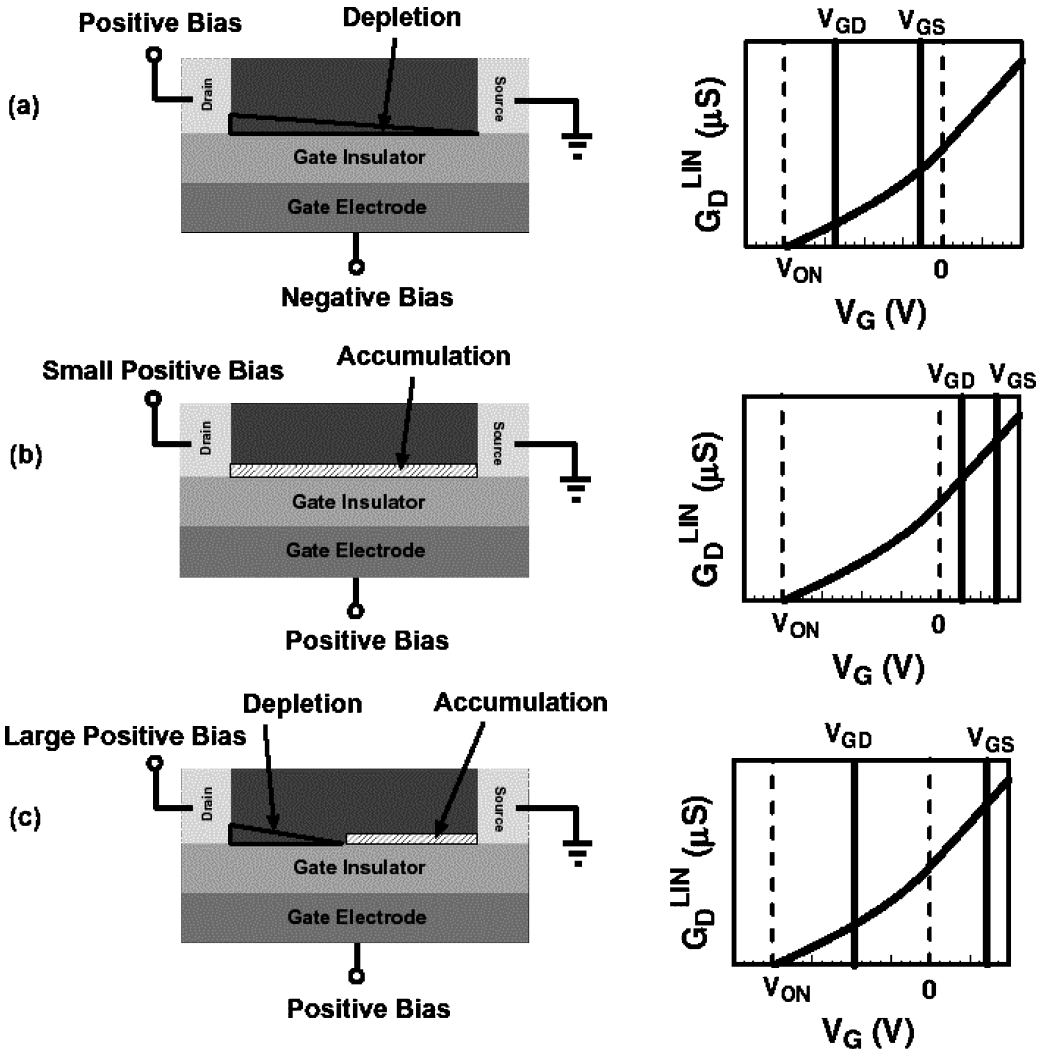

FIG. 4.7. Depletion-mode TFT cross-section and corresponding $G_D^{LIN} - V_G$ plot showing three operating conditions: (a) the channel has a depletion region extending from the source to the drain, (b) the channel has an accumulation region extending from the source to the drain, and (c) the channel is depleted near the drain and is accumulated near the source. The dashed lines separate the regions of operation (i.e., zero, depletion, and accumulation). Thus, the magnitude of V_{GD} and V_{GS} (indicated by the solid lines) with respect to V_{ON} and zero volts determine which operating region applies.

TABLE 4.2(a)
Variable definition for the comprehensive n-channel, depletion-mode TFT model

Variable designation	Equation
Pinch-off voltage	$V_P = -\frac{qN_Dh^2}{2\varepsilon_S}$
Turn-on voltage	$V_{ON} = V_P - \frac{qN_Dh}{C_G}$
Saturation voltage	$V_{DSAT} = V_{GS} - V_{ON}$
Channel conductance	$\sigma = \mu q N_D$
Channel capacitance	$C_S = \frac{\varepsilon_S}{h}$
ACC-DEPL accumulation current	$I_{ACC} = \frac{Z\mu C_G}{2L}V_{GS}^2 + \frac{Zh\sigma}{L}V_{GS}$
ACC-DEPL depletion current	$I_{DEPL} = \frac{Z}{L}\sigma h[(1+\frac{C_S}{C_G})(V_{DS}-V_{GS}) - \frac{2}{3}V_P(\frac{C_S^3}{C_G^3} - (\frac{C_S^2}{C_G^2} + \frac{V_{GD}}{V_P})^{\frac{3}{2}})]$
ACC-DEPL saturation current	$I_{DEPL2} = \frac{Z}{L}\sigma h[(1+\frac{C_S}{C_G})(V_{ON}) - \frac{2}{3}V_P(\frac{C_S^3}{C_G^3} - (\frac{C_S^2}{C_G^2} + \frac{V_{ON}}{V_P})^{\frac{3}{2}})]$

TABLE 4.2(b)
Central equations and model parameters for the comprehensive n-channel, depletion-mode TFT model

Regime of operation	Equation	Constraints
DEPL	$I_D = \frac{Z}{L}\sigma h[(1+\frac{C_S}{C_G})V_{DS} - \frac{2}{3}V_P((\frac{C_S^2}{C_G^2}+\frac{V_{GS}}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P})^{\frac{3}{2}})]$	$V_{ON} < V_{GS} < 0$ $V_{DS} < V_{DSAT}$
DEPL-SAT	$I_D = \frac{Z}{L}\sigma h[(1+\frac{C_S}{C_G})V_{DSAT} - \frac{2}{3}V_P((\frac{C_S^2}{C_G^2}+\frac{V_{GS}}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{ON}}{V_P})^{\frac{3}{2}})]$	$V_{ON} < V_{GS} < 0$ $V_{DS} \geq V_{DSAT}$
ACC	$I_D = \frac{Z}{L}[\mu C_G(V_{GS}V_{DS} - \frac{V_{DS}^2}{2}) + \sigma h V_{DS}]$	$V_{GS} \geq 0$ $V_{DS} < V_{GS}$
ACC-DEPL	$I_D = I_{ACC} + I_{DEPL}$	$V_{GS} \geq 0$ $V_{DSAT} > V_{DS} \geq V_{GS}$
ACC-SAT	$I_D = I_{ACC} + I_{DEPL2}$	$V_{GS} \geq 0$ $V_{DS} \geq V_{DSAT}$
Model parameters	Geometrical-based	Z, L, h, C_G
	Channel-based	N_D,μ, ε_S

Figure 4.9 shows measured $I_D - V_{DS}$ characteristics for a SnO_2 TTFT with a simulated fit using the comprehensive depletion-mode model. Notice that the comprehensive depletion mode-model is able to simulate a wider range of applied gate bias than the 3-layer model fit to the same data shown in Figure 4.5. The small deviation between the bottom simulated curve of Figure 4.9 and the measured data is attributed to the invalid constant mobility assumption employed for this simulation. Measured mobility trends verify this assertion.

An equivalent circuit corresponding to the comprehensive n-channel, depletion-mode model is given in Figure 4.10. Two switches (S_1 and S_2) are used to select which of the three possible channel current paths is operative. Switch S_1 is controlled by V_{GS}, and establishes whether the channel near the source is in accumulation ($V_{GS} > 0$ V) or depletion ($V_{GS} < 0$ V). Switch S_2 depends on $V_{GD,}$ and determines whether the channel near the drain is in accumulation ($V_{GD} > 0$) or depletion ($V_{GD} < 0$). The current path on the left corresponds to the ACC regime ($V_{GS} > 0$ V and $V_{GD} > 0$ V), which includes a bulk resistance in parallel with the gate-induced current; this operating regime is equivalent to the 3-layer model (if surface conduction is neglected). The middle path corresponds to the ACC-DEPL regime ($V_{GS} > 0$ V and $V_{GD} < 0$ V). Finally, the path to the right corresponds to the DEPL regime ($V_{GS} < 0$ V and $V_{GD} < 0$ V).

It can be shown that the comprehensive n-channel, depletion-mode TFT model simplifies to the square-law model in the limit

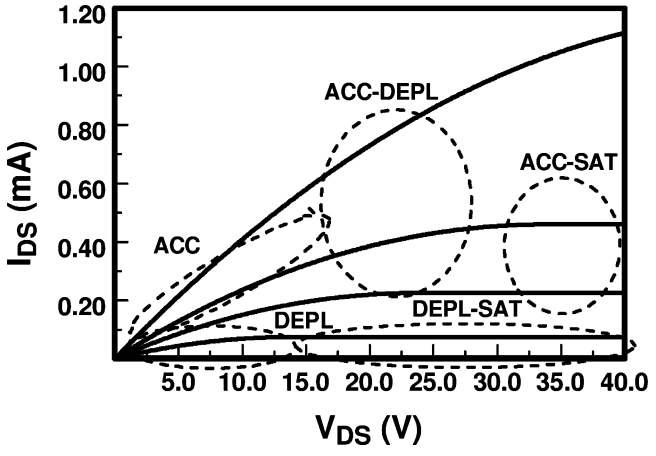

FIG. 4.8. $I_D - V_{DS}$ characteristic simulated using the comprehensive depletion-mode TFT model of Table 3.1 using the model parameters listed in Table 3.2. The five regimes of device operation are indicated. V_{GS} is decreased from 30 V (top curve, showing maximum current) to -10 V in 10 V steps. Model parameters used in this simulation: $Z/L = 10$, $h = 80$ nm, $C_G = 1.7 \times 10^{-9}$ F/cm^2, $\mu = 5$ cm^2/V-s, and $N_D = 3 \times 10^{17}$ cm^{-3}.

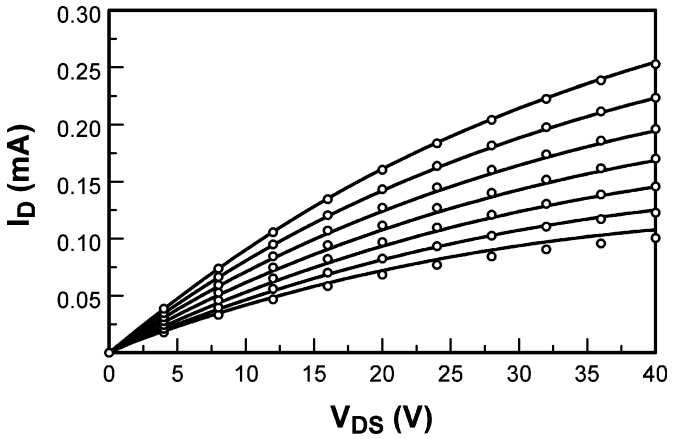

FIG. 4.9. Measured $I_D - V_{DS}$ curves (open circles) for a SnO_2 TTFT with a fit to the data (continuous lines) using the depletion-mode model. V_{GS} is decreased from 20 V (top curve, showing maximum current) to -10 V in 5 V increments. Model parameters used in this simulation: $N_D = 2.2 \times 10^{18}$ cm$^{-3,}$ $Z/L = 5$, $h = 60$ nm, $C_G = 7 \times 10^{-8}$ F/cm^2, and $\mu = 0.3$ cm^2/V-s.

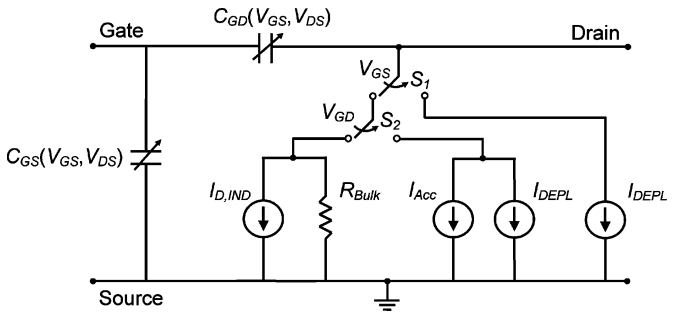

FIG. 4.10. An equivalent circuit for the comprehensive n-channel, depletion-mode model. The switches S_1 and S_2 establish which of the three channel current paths is operative, based on the magnitude and polarity of V_{GS} and V_{GD}.

$C_S \gg C_G$. There are several ways to justify the limit $C_S \gg C_G$. Perhaps the simplest justification involves recognizing that if this limit is satisfied, all of the voltage applied to the gate of the TFT is dropped across the insulator. This implies that the charge induced in the channel is equal to $C_G(V_{GS} - V_{ON})$ so that

$$G_D^{LIN} = \frac{Z}{L} C_G \left(V_{GS} - V_{ON}\right), \qquad [4.5]$$

which is identical to Eq. 10.16, which is used to derive the square-law model, except that V_T is replaced by V_{ON}.

V. DISCRETE TRAP MODEL

The objective of this section is to present an overview of the discrete trap model and to elucidate the primary device physics consequences of carrier trapping. The initial portion of this derivation was previously introduced by Sze.[3]

A. Model Overview

Although it is more likely that there is a distribution of traps over a specific energy range, a discrete trap is used here to simplify mathematical analysis and to provide insight with regard to the effect of traps on TFT performance. The discrete trap under consideration in this model is assumed to interact only with conduction band electrons, not valence band holes. Therefore, it is characterized by its ionization energy, E_T, capture cross-section, σ_n, and density, N_T.

Assuming that the average conduction band electron velocity and capture cross-section is constant, the rate of conduction band trapping is a function of the empty trap density and the density of electrons present in the conduction band. In contrast, the rate of emission from the trap state to the conduction band is a function of the filled trap density and the conduction band electron density when the Fermi-level, E_F, is equal E_T. Mathematically, the rate of conduction band trapping is expressed as, $\bar{v}\sigma_n \left(N_T - n_t\right) n_c$, where $\bar{v}$ is the average conduction band electron velocity, $(N_T - n_t)$ is the density of empty traps, and n_c is the density of electrons present in the conduction band. The rate of electron emission from the trap state to the conduction band is expressed as, $\bar{v}\sigma_n n_t n_1$, where n_1 is the conduction band electron density when $E_F = E_T$ and is given by

$$n_1 = N_c e^{\left(\frac{-E_T}{k_B T}\right)}, \qquad [5.1]$$

where N_c is the effective density of states of the conduction band and k_B is Boltzmann's constant.

When considering the $Q = C \times V$ relationship for the discrete trap model, it is important to recognize that the total charge induced in the channel by the application of a gate voltage is distributed into both conduction band and trap states,

$$\begin{aligned} q\left(\Delta n_c + \Delta n_t\right) &= q\left[\left(n_c + n_t\right) - \left(n_{co} + n_{to}\right)\right] \\ &= \frac{C_G}{h}\left[V_{GS} - V\left(y\right)\right], \end{aligned} \qquad [5.2]$$

where n_{co} and n_{to} are initial, zero-bias densities of free conduction band electrons and trapped electrons, respectively. Rearrangement of Eq. 5.2 leads to

$$q\left(n_c + n_t\right) = \frac{C_G}{h}\left[V_{GS} - V\left(y\right) - V_{ON}\right], \qquad [5.3]$$

where V_{ON}, the turn-on voltage, is given by

$$V_{ON} = -\frac{qh}{C_G}\left(n_{co} + n_{to}\right). \qquad [5.4]$$

Using Eq. 5.2 in conjunction with the steady-state assumption (i.e., the conduction band trapping rate is equivalent to the trap emission rate), the voltage along the channel can be solved for and integrated to determine the drain current, as shown in section X.C.

Table 5.1 summarizes the TFT discrete trap model. Note that the V_{DS} and V_{GS} constraint equations, the V_{DSAT} pinch-off equation, and the geometrical and channel-related model parameters are all identical to those employed in the square-law model. In

TABLE 5.1
A summary of the discrete trap model

Variable designation		Equation
Turn-on voltage		$V_{ON} = -\frac{qh}{C_G}(n_{co} + n_{to})$
Pinch-off condition		$V_{DSAT} = V_{GS} - V_{ON}$
Regime of operation	Equation	Constraints
Cut-off	$I_D = 0$	$V_{GS} < V_{ON}$
Pre-pinch-off	Appendix (X.C); Eq. 10.53	$V_{GS} \geq V_{ON}$ $V_{DS} \leq V_{DSAT}$
Post-pinch-off	Appendix (X.C); Eq. 10.55	$V_{GS} \geq V_{ON}$ $V_{DS} > V_{DSAT}$
Model parameters	Geometrical-based	Z, L, h, C_G
	Channel-based	μ, n_{co}
	Trap-related	N_T, E_T, n_{to}
	Physical	T

contrast, the pre-pinch-off and the post-pinch-off model equations, which are derived in section X.C, are more complex due to the inclusion of discrete trap effects.

B. Simulation Results: Subthreshold Current Considerations

The previously discussed models have not explicitly considered the threshold voltage, V_T, or subthreshold current, that is, the drain current obtained when the gate voltage is less than V_T. Before considering subthreshold current, V_T must be clearly considered and established. Here, V_T is a demarcation point, establishing the onset of subthreshold current. Additionally, V_T is sometimes used to quantify the onset of drain current conduction.

When considering V_T and V_{ON}, their relative effectiveness as drain current onset parameters is an issue. Figure 5.1 illustrates the estimation of V_T via simple linear extrapolation of an $I_D - V_{GS}$ transfer curve for a prototypical zinc tin oxide TFT. As shown, the extrapolated value of V_T is ~5 V. Now, consider V_{ON}, which is evaluated using a $log(I_D) - V_{GS}$ transfer, as shown in Figure 5.2, and results in a value of -4 V for the same device. V_{ON} corresponds to the initial onset of appreciable drain current measured on a $log(I_D) - V_{GS}$ transfer curve. This drain current onset occurs when I_D is larger than the gate leakage and/or the noise floor, which is established by the device under test and the precision of the measurement instrumentation. It is apparent from Figure 5.2 that V_{ON} is a more precise parameter to quantify drain current onset than V_T.[25] Thus, the authors propose the use of V_{ON} as the preferred drain onset device electrical parameter.

The other parameters labeled in Figure 5.2 are the S parameter and the drain current on-to-off ratio. S is typically referred to as the subthreshold swing, which is given by $S = \frac{\partial V_{GS}}{\partial \log(I_D)}|_{\min}$, and characterizes the effectiveness of the gate voltage in reducing the drain current to zero. A small value of S is desirable because this corresponds to a very sharp transition from on to off. The drain current on-to-off ratio, $I_D^{on\text{-}off}$, is established by the maximum drain current and the gate leakage/noise floor. A large $I_D^{on\text{-}off}$ is desirable, because this corresponds to a more effective switch.

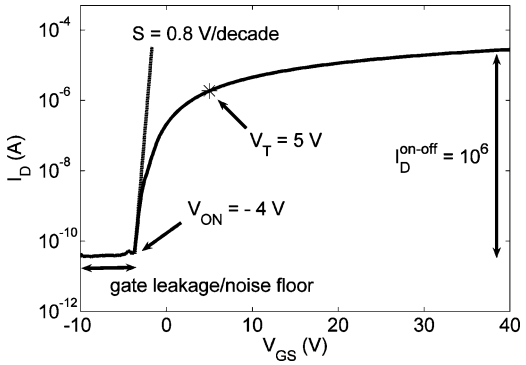

FIG. 5.2. $Log(I_D) - V_{GS}$ transfer curve for a zinc tin oxide, n-channel TFT. The voltage at which the TFT turns on is -4 V. The previously extracted value of the threshold voltage, $V_T =$ 5 V does not correspond to any obvious drain current onset. Geometrical parameters for this TFT are $Z/L = 5{:}1$ and $C_G = 3.45 \times 10^{-8}$ F/cm^2.

Now, consider the ideal $log(I_D) - V_{GS}$ transfer curve shown in Figure 5.3. Note that "ideal" refers to use of the ideal square-law model, neglecting the effect of traps and of diffusion current in establishing the subthreshold current. $V_T = V_{ON}$, $S = 0$, and $I_D^{on\text{-}off} = \infty$ are obtained for the ideal square-law model, as indicated in Figure 5.3. Ideal values for V_T and S are obtained because electron trapping in the channel and/or at channel interfaces is neglected. Moreover, S = 0 for this ideal TFT, whereas S can only be as low as 60 mV/decade for a MOSFET, in which

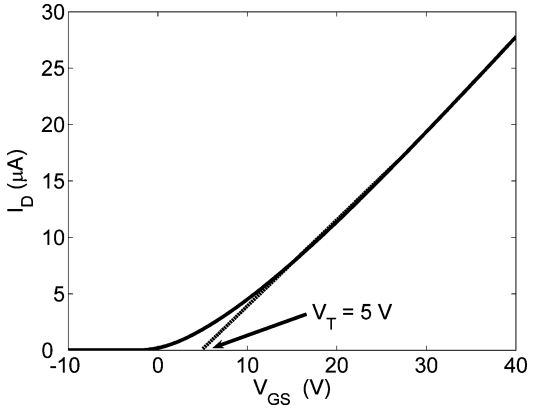

FIG. 5.1. Drain current-gate voltage ($I_D - V_{GS}$) transfer curve for a zinc tin oxide, n-channel TFT. The threshold voltage is estimated to be ~5 V via extrapolation of the linear portion of this curve. Geometrical parameters for this TFT are $Z/L = 5{:}1$ and $C_G = 3.45 \times 10^{-8}$ F/cm^2.

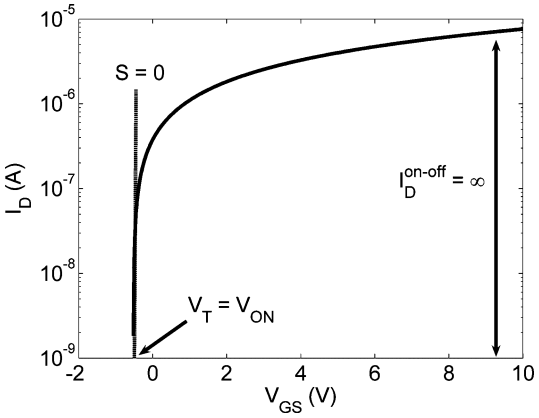

FIG. 5.3. Log $(I_D) - V_{GS}$ transfer curve simulation using the square-law model. In this ideal case, S = 0 V/decade, $V_T = V_{ON}$, and the drain current on-to-off ratio is infinite. For this simulation $V_{DS} = 100$ mV, $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_o = 1 \times 10^{17}$ cm^{-3}.

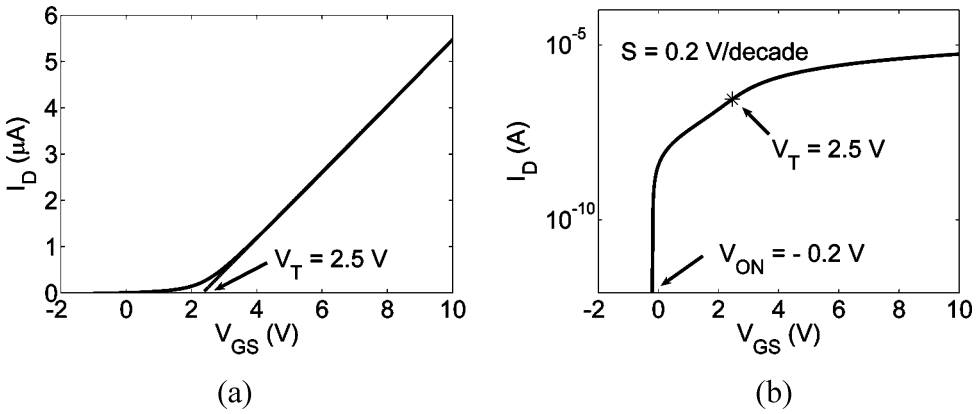

FIG. 5.4. $I_D - V_{GS}$ and $log(I_D) - V_{GS}$ transfer curves simulated using the discrete trap model. For this simulation, T = 300 K, $V_{DS} = 1$ V, $N_T = 5 \times 10^{17}$ cm^{-3}, $E_T = 0.15$ eV below the conduction band minimum, $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

subthreshold current is modeled as diffusion current.[26] $I_D^{on\text{ - }off}$ is infinite because the ideal square-law model ignores gate leakage and instrumentation noise. Thus, assessment of S and $I_D^{on\text{ - }off}$ require "real world" considerations involving traps and gate leakage/measurement noise to be taken into account.

Figure 5.4 shows simulated $I_D - V_{GS}$ and $log(I_D) - V_{GS}$ transfer curves for a TFT using the discrete trap model. From Figures 5.4(a) and 5.4(b), V_T is estimated via linear extrapolation as ∼2.5 V and V_{ON} is estimated to be approximately −0.2 V, respectively.

Recall that the turn-on voltage is given by

$$V_{ON} = -\frac{qh}{C_G}(n_{co} + n_{to}), \qquad [5.5]$$

where n_{co} and n_{to} correspond to the density of conduction band electrons and occupied trap states at zero bias. Because n_{co} is chosen to be low, V_{ON} is quite small for this simulation, that is, V_{ON} is ∼–0.2 V. A negative value of V_{ON}, as seen in this case, requires that a negative gate voltage must be applied to remove free and trapped electrons from the channel.

V_T can also be quantitatively defined within the context of the discrete trap model. Based on the discrete trap model, V_T is equivalent to the gate voltage required to fill all traps. This V_T is given by,

$$V_T = \frac{qh}{C_G}(N_T - n_{to}) + \frac{qh}{C_G}(n_1 - n_{co}) \qquad [5.6a]$$

$$= V_{TRAP} + V_{ELECTRON}. \qquad [5.6b]$$

V_T is composed of two constituents, V_{TRAP} and $V_{ELECTRON}$. V_{TRAP} is associated to the gate voltage required to fill the empty traps, $(N_T - n_{to})$. However, V_{TRAP} neglects the change in conduction band electron density with applied gate voltage. This change is accounted for with $V_{ELECTRON}$. Moreover, evaluating Eq. 5.6a using simulation parameters yields $V_T = 2.5$ V, which is equivalent to the estimate obtained from linear extrapolation of Figure 5.4(a).

Returning to Figure 5.4(b), as the gate voltage increases above V_{ON}, the drain current increases abruptly with an extremely large slope. As E_F moves closer to E_C and E_T, the steady-state trap occupancy increases, because $E_T - E_F$ decreases. Thus, between V_{ON} and V_T, that is, $-0.2 \leq V_{GS} \leq 2.5$ V, the slope of the $log(I_D) - V_{GS}$ curve is controlled by the rate of steady-state trapping and results in a non-zero value of S; for the simulation shown in Figure 5.4(b), S is ∼0.2 V/decade. At gate voltages greater than V_T, the Fermi level moves above the trap level, so that $E_T - E_F$ is negative and essentially all the traps are filled. Any further increase in the gate voltage results in further accumulation of free electrons in the conduction band, corresponding to TFT operation without the influence of traps.

Comparing the $\log(I_D) - V_{GS}$ plots for a real TFT and a simulated TFT with a discrete trap, as shown in Figures 5.2 and 5.4(b), respectively, it is apparent that the simulated curve is dissimilar to the measured curve (i.e., the simulated curve has a kink in the current near V_T). This discrepancy is likely due to the discrete trap assumption (which is employed for computational simplicity); it is likely that there is a distribution of traps over a specific energy range.

Simulated $log(I_D) - (V_{GS} - V_{ON})$ transfer characteristics for three trap densities with a constant trap depth (i.e., $E_T \sim -0.15$ eV) are shown in Figure 5.5. For a trap density of 1×10^{15} cm^{-3}, V_{TRAP} is negligible. Thus, the corresponding $log(I_D)$ curve is close to that of an ideal TFT with no traps. However, as N_T is increased, the drain current degrades. Correspondingly, V_{TRAP} and S increase with increasing trap density; $V_{TRAP} - V_{ON} \sim 0.08$, 3.8, and 10.7 V and S ∼0.01, 0.3685, and 1.46 V/decade for $N_T = 1 \times 10^{15}$, 7×10^{17}, and 2×10^{18} cm^{-3}, respectively. S as a function of N_T is shown in Figure 5.6; S is initially very small for trap densities less than 1×10^{17} cm^{-3}, but increases significantly thereafter.

The dependence of E_T on S is shown in Figure 5.7 via simulation using the discrete trap model. For this simulation $E_F = 0.21$ eV below the conduction band, as established by n_{co}. As

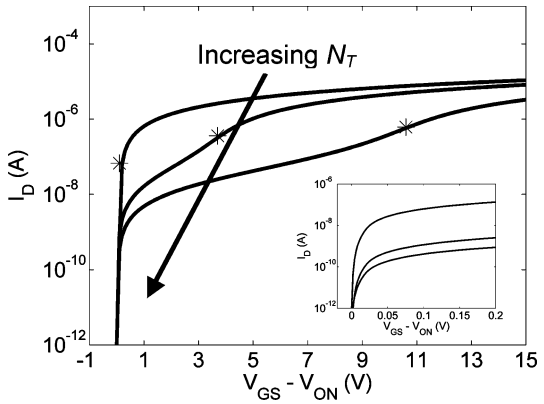

FIG. 5.5. Simulated $log(I_D) - (V_{GS} - V_{ON})$ transfer curves as a function of trap density, N_T, for a TFT using the discrete trap model. The arrow indicates the direction of increasing N_T. These curves correspond to N_T values of 1×10^{15}, 7×10^{17}, and 2×10^{18} cm^{-3} and V_{ON} values of -0.54, -3.8, -10 V, respectively. V_{TRAP} is represented by "*" on each $log(I_D)$ curve. (Inset) The transfer characteristic near $V_{GS} - V_{ON} = 0$ V is shown in the inset. For these simulations, $V_{DS} = 1$ V, $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{17}$ cm^{-3}.

shown in Figure 5.7, S is small for shallow traps and increases near E_F, but then decreases then decreases beyond E_F. This relationship between S and E_T is attributed to the trap re-emission rate and occupancy, as discussed in the following.

Figure 5.8 shows an energy band diagram of the upper band portion of a semiconductor at flat-band with three discrete traps at E_{T1}, E_{T2}, and E_{T3} with respect to the conduction band minimum, E_C. E_F establishes trap occupancy. As indicated in Figure 5.8, the deepest trap at energy E_{T3} is almost completely filled with electrons, because it is located below E_F. In contrast, the shallowest trap at E_{T1} traps very few electrons in steady-state

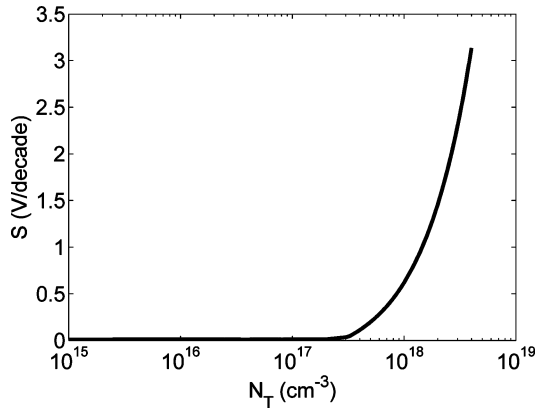

FIG. 5.6. Simulated S as a function of N_T using the discrete trap model with a constant trap depth of $E_C - E_T = 0.15$ eV. For this simulation, $V_{DS} = 1$ V, $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

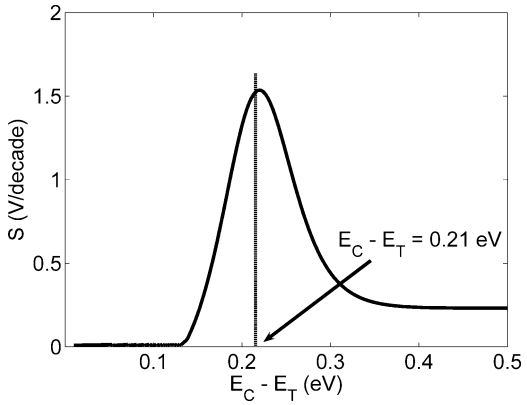

FIG. 5.7. Simulated S as a function of trap depth, $E_C - E_T$, at a constant trap density of 5×10^{17} cm^{-3}. For this simulation, $V_{DS} = 1$ V, $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

because its shallow energy depth corresponds to it having a very large thermal emission rate, as given by

$$e_n = \sigma_n \upsilon_{th} N_c e^{-E_T/k_B T}, \qquad [5.7]$$

where υ_{th} is the thermal velocity. Thus, a deeper trap has a smaller trap re-emission rate and, hence, a larger steady-state occupancy than an otherwise identical but shallower trap; this translates into less drain current due to more trapping for a deeper trap (so long as E_T is above E_F). In the context of the S trend shown in Figure 5.7, a deeper trap (up to E_F) translates to a degradation (increase) in S due to a lower trap re-emission rate. Beyond E_F, S improves (decreases) with E_T, as a larger percentage of traps are occupied for deeper traps.

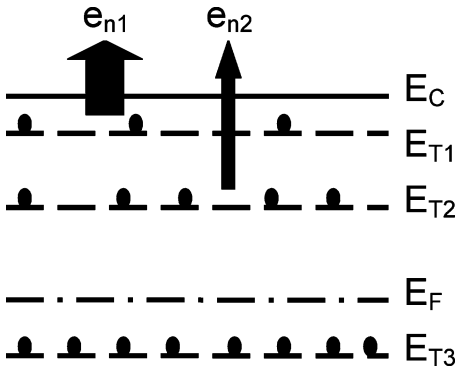

FIG. 5.8. Energy-band diagram of the upper band gap portion of the semiconductor at flat band. Three discrete traps are present at E_{T1}, E_{T2}, and E_{T3} with respect to the conduction band minimum, E_C. E_F determines the trap occupancy, which is qualitatively indicated by the fraction of the trap states occupied by electrons (filled circles). The widths of the arrows represent the relative rate of trap emission.

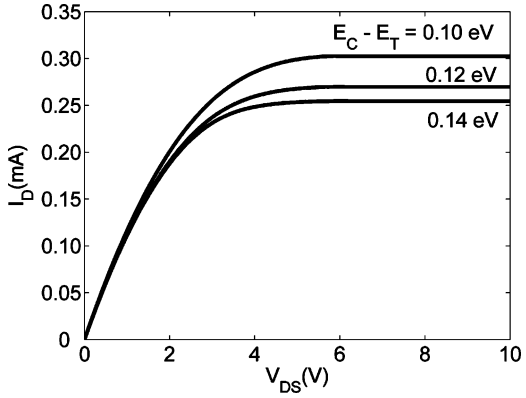

FIG. 5.9. Drain current-drain voltage ($I_D - V_{DS}$) characteristics for an n-channel TFT corresponding to a gate voltage of 6 V and a trap density of $N_T = 5 \times 10^{17}$ cm^{-3}. The Fermi level, E_F, as established by the initial free carrier concentration, n_{co}, is $E_C - E_F = 0.21$ eV. Geometrical and channel-based parameters employed for this simulation are: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

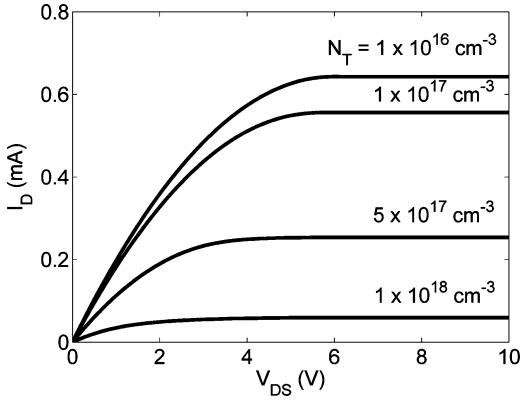

FIG. 5.10. Drain current-drain voltage ($I_D - V_{DS}$) characteristics for an n-channel TFT corresponding to a gate voltage of 6 V and a trap depth of $E_C - E_T = 0.15\ eV$ below the conduction band minimum. Geometrical and channel-based parameters employed for this simulation are: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

C. Simulation Results: Above-Threshold Effects of Trap Density and Energy Depth

Figure 5.9 demonstrates that the energy depth of a trap, E_T, affects the TFT $I_D - V_{DS}$ characteristics. When E_T is between E_C and E_F, a deeper trap results in a larger reduction in the drain current, as shown in Figure 5.9. Although it is not shown in Figure 5.9, when E_T drops below E_F, there is minimal effect on I_D. The decrease in the drain current with increasing trap depth as shown in Figure 5.9 is attributed to a decrease in the rate of trap re-emission, as previously discussed in the context of Figure 5.8.

Figure 5.10 illustrates the output $I_D - V_{DS}$ curves for different values of N_T at $V_{GS} = 6$ V and a trap depth of 0.15 eV below the conduction band minimum. A decrease in the drain current with increasing trap density, N_T, is observed in Figure 5.10. An increase in N_T causes an increase in n_t, thereby reducing the free electron concentration available for conduction and thus reducing the drain current. Moreover, a decrease in the free electron concentration translates into a corresponding decrease in the slope of the I_D curve in the pre-pinch-off regime. A decrease in the I_D slope at small V_{DS}, as shown in Figure 5.10, indicates that the average channel mobility deteriorates as the trap density increases.

Mobility trends in the context of the discrete trap model are more fully discussed in section VI.E.

VI. MOBILITY

In its most general sense, mobility, μ, is a linear proportionality constant relating the carrier drift velocity, v_d, to the applied electric field, ξ, that is,

$$v_d = \mu\xi. \qquad [6.1]$$

Up to now, the channel mobility of a TFT has been treated as a constant. Physically, there are various reasons why the channel mobility may not be constant (e.g., interface roughness scattering, velocity saturation, and electron trapping), but instead, can vary with V_{DS} and especially with V_{GS}.[27–29] An ideal TFT would have a constant mobility, independent of V_{GS}. In contrast, the mobility of a real TFT usually increases above threshold, and then either saturates or peaks and decreases as V_{GS} increases.

A. Effective and Field-Effect Mobilities

The channel mobility dependence on voltage leads to the definition of several different kinds of mobilities, which are distinguished by the procedure employed for their estimation from measured data. Effective mobility, μ_{EFF}, and field-effect mobility, μ_{FE}, are the two most commonly employed TFT mobilities. Effective mobility, μ_{EFF}, is extracted from the drain conductance, g_d, measured in the linear regime of operation.

Figure 6.1 illustrates the linear regime of operation of an $I_D - V_{DS}$ plot for a specific V_{GS}. It is evident from this curve that linear regime is defined with respect to V_{DS}. Employing the pre-pinch-off square-law model of section III.A as a starting point, if V_{DS} is very small (i.e., if $V_{DS} \to 0$ V), then an approximation for I_D in the linear regime is,

$$I_D \approx \frac{Z\mu C_G}{L}\left[(V_{GS} - V_T)V_{DS}\right]. \qquad [6.2]$$

Note here that V_T is used instead of V_{ON} so as to follow the classical formulation of μ_{EFF} and μ_{FE}. Differentiating Eq. 6.2 with respect to V_{DS} yields,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \approx \frac{Z\mu C_G}{L}\left(V_{GS} - V_T\right). \qquad [6.3]$$

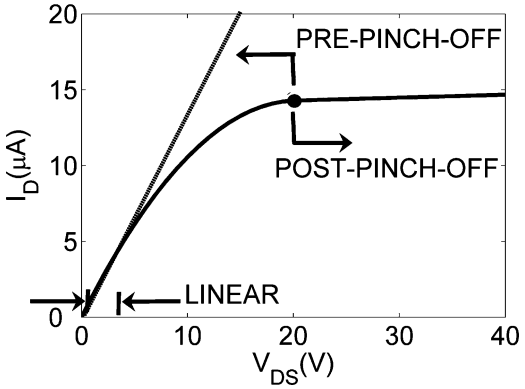

FIG. 6.1. Simulated $I_D - V_{GS}$ characteristics for an n-channel TFT generated using the square-law model. The straight line identifies the linear regime. Square-law model parameters employed for this simulation are: $V_{ON} = -5$ V, $C_G = 70$ nF/cm^2, $\mu = 30$ cm^2/V-s, and Z/L = 10.

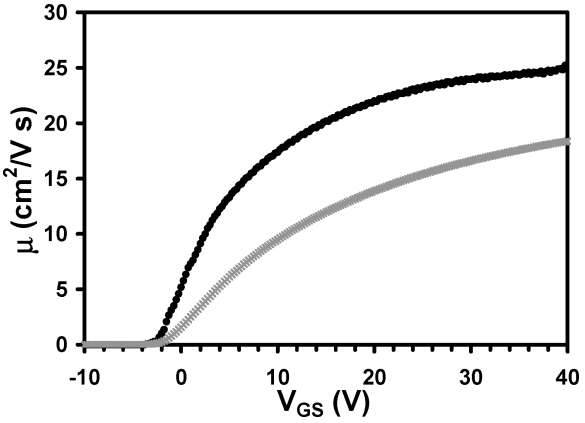

FIG. 6.2. Extracted mobilities, μ_{AVG} (gray) and μ_{INC} (black), for a zinc tin oxide TFT with $V_{DS} = 100$ mV.

Solving Eq. 6.3 for mobility and identifying this as the effective mobility yields,

$$\mu_{EFF} = \frac{g_d}{\frac{Z}{L} C_G (V_{GS} - V_T)}. \quad [6.4]$$

In contrast to μ_{EFF}, which is obtained from g_d, the field-effect mobility, μ_{FE}, is derived from the transconductance, g_m. Again starting with Eq. 6.2, but this time differentiating with respect to V_{GS} yields,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \frac{Z \mu C_G}{L} V_{DS}. \quad [6.5]$$

Solving for what is now denoted field-effect mobility gives,

$$\mu_{FE} = \frac{g_m}{\frac{Z}{L} C_G V_{DS}}. \quad [6.6]$$

Equations 6.4 and 6.6 constitute the defining relations for effective and field-effect mobility, respectively. Note that the gate voltage dependence of the effective mobility depends explicitly on the gate voltage and implicitly on the drain conductance, whereas the field-effect mobility depends implicitly on the gate voltage g_m, that is, $\mu_{EFF}(V_{GS}) = f[V_{GS}, g_d(V_{GS})]$ and $\mu_{FE}(V_{GS}) = f[g_M(V_{GS})]$.

B. Average and Incremental Mobilities

Although μ_{EFF} and μ_{FE} are extensively employed in the technical literature as estimators of TFT channel mobility, a better approach is to use average and incremental mobility, μ_{AVG} and μ_{INC}, respectively, for channel mobility assessment. Our preference is based on the fact that μ_{AVG} and μ_{INC} have precise physical interpretations, whereas μ_{EFF} and μ_{FE} do not.[25]

The defining relation for the average mobility is similar to Eq. 6.4, which is used to define μ_{EFF} except that V_T, is replaced by V_{ON}, yielding,

$$\mu_{AVG} = \frac{g_d}{\frac{Z}{L} C_G (V_{GS} - V_{ON})}. \quad [6.7]$$

μ_{AVG} physically corresponds to the average mobility of the *total* carrier concentration in the channel.

The defining relation for the incremental mobility, μ_{INC}, is,

$$\mu_{INC} = \frac{\frac{\partial g_d}{\partial V_{GS}}}{\frac{Z}{L} C_G}. \quad [6.8]$$

In contrast to μ_{AVG}, μ_{INC} physically corresponds to the mobility of the carriers that are incrementally added to the channel as the gate voltage incrementally increases in magnitude. This physical interpretation is based on the assumption that the mobility of carriers already present in the channel does not change.

To better appreciate the physical significance of μ_{AVG} and μ_{INC}, consider the measured mobility data of a zinc tin oxide TFT, as presented in Figure 6.2. Beginning at V_{ON}, which is approximately equal to -3.8 V, the incremental mobility begins to increase. The low mobility near the turn-on voltage is a result of the fact that most of the initial carriers injected from the source into the channel are trapped in interface states and/or in "bulk" channel layer traps. As V_{GS} increases, these traps are filled, such that a smaller fraction of the incrementally added carriers are trapped. The incremental mobility continues to increase as V_{GS} increases until it either saturates or where second-order effects such as series resistance or interface roughness scattering are no longer negligible and μ_{INC} begins to decrease. The important point is to recognize that the μ_{INC} trend with respect to V_{GS} is reflective of the mobility of carriers added incrementally to the channel.

The average mobility trend with respect to V_{GS}, as shown in Figure 6.2, provides an equally interesting result. $\mu_{AVG}(V_{GS})$ is a moving average of μ_{INC} from V_{ON} to V_{GS}.[25] μ_{AVG} is usually lower in value than μ_{INC} because it represents the average mobility of all of the carriers in the channel, including carriers localized in traps.

As a figure-of-merit, μ_{AVG} provides a better predictor of device performance for circuit applications because it takes into account all of the carriers in the channel. In contrast, μ_{INC} is

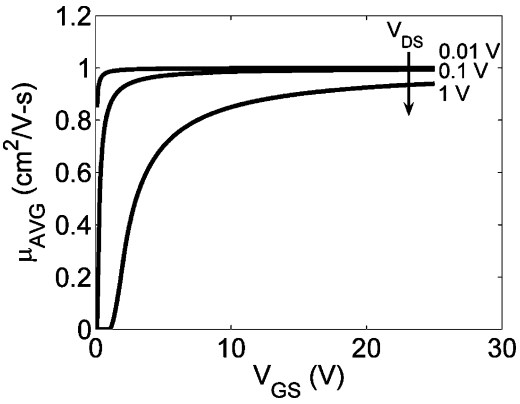

FIG. 6.3. μ_{AVG}, extracted from an ideal $I_D - V_{GS}$ curve simulated using the square-law model. Starting with the upper curve, V_{DS} is 0.01, 0.1, 1 V, for each subsequent μ_{AVG} curve. Model parameters used for this simulation: $V_{ON} = 0$ V, Z/L = 10, h = 100 nm, $C_G = 7 \times 10^{-7}$ F/cm^2, $n_0 = 10^{14}$cm^{-3}, and $\mu_{MODEL} =$ 1 cm^2/V-s.

of greater physical significance, as it is more directly correlated with the transport physics of carriers in the channel.

For further consideration, Ref. 25 provides a more in-depth mathematical derivation and explanation of μ_{INC} and μ_{AVG}.

C. Simulation Results: Ideal Mobility Extraction

In the ideal square-law model, mobility is assumed to be constant with respect to V_{GS}. Thus, according to this model, a plot of mobility versus V_{GS} should result in a step function increase in mobility, from zero to its full value occurring at V_{ON}. Figure 6.3 shows $\mu_{AVG} - V_{GS}$ curves which are extracted from an ideal $I_D - V_{GS}$ curve that are simulated using the ideal square-law model with $\mu_{MODEL} = 1$ cm^2/V-s. The important lesson to learn from Figure 6.3 is that μ_{AVG} cannot be accurately extracted, even from an ideal $I_D - V_{GS}$ curve, unless this extraction occurs at a sufficiently small value of V_{DS}. A corresponding mobility extraction artifact is also present in a $\mu_{INC} - V_{GS}$ curve if V_{DS} is too large, but is less pronounced than in a $\mu_{AVG} - V_{GS}$ curve. These mobility extraction artifacts arise as a result of a breakdown in the assumption of linearity employed in Eq. 6.2.

When V_{GS} is near V_{ON}, the linearity condition, $V_{DS} \ll V_{GS} - V_{ON}$, is no longer satisfied. Beginning with the definition of average mobility in Eq. 6.7 and noting that $g_d = \frac{\partial I_D}{\partial V_{DS}}$, the average mobility can be expressed as,

$$\mu_{AVG} = \frac{\frac{\partial I_D}{\partial V_{DS}}}{\frac{Z}{L} C_G (V_{GS} - V_{ON})}. \qquad [6.9]$$

If the linearity condition is not met, the partial derivative term constituting the numerator of Eq. 6.9 must be assessed by differentiating the square-law model pre-pinch-off regime I_D expression (i.e., Eq. 2.1) with respect to V_{DS}, resulting in,

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_{MODEL} C_G Z}{L} (V_{GS} - V_{ON} - V_{DS}). \qquad [6.10]$$

Inserting Eq. 6.10 into Eq. 6.9 and canceling terms yields,

$$\mu_{AVG} = \mu_{MODEL} \frac{(V_{GS} - V_{ON} - V_{DS})}{(V_{GS} - V_{ON})}. \qquad [6.11]$$

Equation 6.11 provides a quantitative means of estimating the extent of the mobility extraction artifact. It can be seen that for values of V_{GS}–$V_{ON} \gg 0V_{DS}$, $\mu_{AVG} \approx \mu_{MODEL}$. Also, note that when V_{GS}–$V_{ON} = V_{DS}$, $\mu_{AVG} = 0$. This analysis demonstrates that accurate mobility extraction requires the use of the smallest possible value of V_{DS}.

D. Apparent Mobility Degradation due to Series Resistance

Real TFT curves exhibit non-idealities that are manifest as a non-abrupt increase in mobility with increasing V_{GS} at low V_{GS} or a decrease in mobility at high V_{GS}. There are two primary potential causes of a decrease in mobility at high V_{GS}, interface roughness scattering and series resistance. Series resistance leads to a reduction in the "apparent" mobility, as presented in this section.

Figures 6.4 illustrates the effect of series resistance on the apparent incremental as a function of V_{GS}. Figure 6.4 shows a general trend with the apparent incremental mobility increasing above the turn-on voltage, peaking, and then degrading. The degradation effect is due to the fact that an appreciable fraction of the applied voltage is dropped across the series resistors R_S and R_D. As the series resistance increases, the percentage of the applied voltage dropped across R_S and R_D increases, resulting in less current conduction and, hence, a lower apparent incremental mobility.

The mobility versus V_{GS} trends shown in Figure 6.4 are not representative of the true mobility of the carriers in the channel but, rather, constitute an artifact associated with series resistance. An example of a mobility degradation effect where the degraded mobility is indicative of the true mobility of the carriers

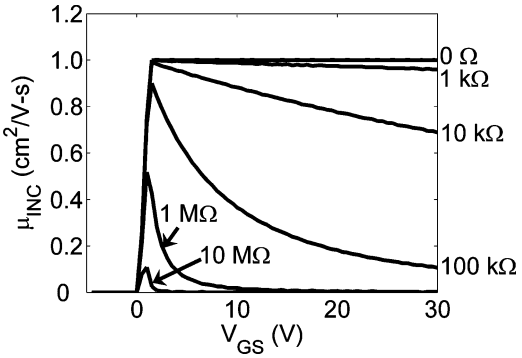

FIG. 6.4. Simulated incremental mobility $- V_{GS}$ characteristics for varying values of series resistance. Model parameters used for this simulation: Z/L = 10, h = 100 nm, $C_G = 7 \times 10^{-7}$ F/cm^2, $n_0 = 10^{14}$ cm^{-3}, and $\mu = 10$ cm^2/V-s. R_{SERIES} = [0 Ω, 1 kΩ, 10 kΩ, 100 kΩ, 1 MΩ, 10 MΩ]. Note that $R_{SERIES} = R_S + R_D$ and $R_D = R_S$.

in the channel would be interface roughness scattering. This mobility degradation mechanism occurs when carriers, under a large gate-to-source voltage, are pulled close to a rough insulator/semiconductor interface. Scattering occurs because these carriers interact with the uneven interface, thereby lowering their velocities and, therefore, their mobilities.[29]

E. Mobility Degradation due to a Discrete Trap

This subsection explores the effects of traps on the apparent average and the incremental mobility. μ_{AVG} and μ_{INC} are extracted from $I_D - V_{GS}$ curves simulated using the discrete trap model.

$\mu_{INC} - (V_{GS} - V_{ON})$ curves as a function of trap density, N_T, are shown in Figure 6.5. As discussed previously μ_{INC} is a measure of the mobility of carriers differentially induced into the channel by an incremental increase in the gate voltage. The $\mu_{INC} - (V_{GS} - V_{ON})$ curve transition for $N_T = 1 \times 10^{16}$ cm^{-3} is very close to an ideal step-function transition to the bulk mobility. As N_T increases, a $\mu_{INC} - (V_{GS} - V_{ON})$ curve shifts along the V_{GS} axis and the transition is less abrupt. The voltage, V_{TRAP}, below which the majority of the gate voltage induced electrons are trapped is indicated by "*" on each of the $\mu_{INC} - (V_{GS} - V_{ON})$ curves shown in Figure 6.5.

Figure 6.6 shows simulated $\mu_{INC} - (V_{GS} - V_{ON})$ curves as a function of trap depth at a constant trap density of 5×10^{17} cm^{-3}. The important trend indicated in Figure 6.6 is that the abruptness of the transition in a $\mu_{INC} - (V_{GS} - V_{ON})$ curve is steeper for a deeper trap than for a shallow trap. When a deep trap

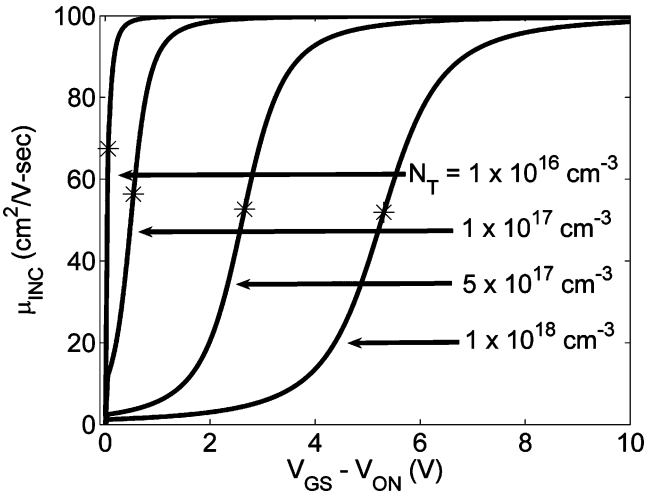

FIG. 6.5. Simulated $\mu_{INC} - (V_{GS} - V_{ON})$ characteristics as a function of trap density, N_T for a trap depth $E_C - E_T = 0.15$ eV and a drain voltage $V_{DS} = 0.2$ V. The asterisk (*) on each $\mu_{INC} - V_{GS}$ curve corresponds to the voltage, V_{TRAP}, that acts as the "mobility threshold voltage" value below which most of the induced electrons occupy the trap states. Model parameters used for this simulation: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu_{MODEL} = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

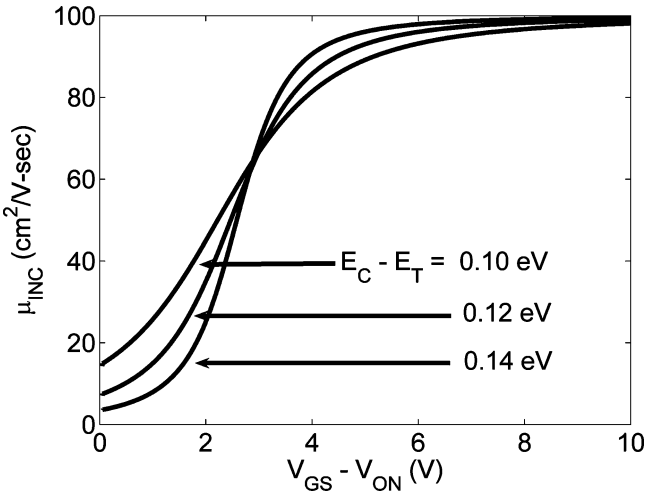

FIG. 6.6. Simulated $\mu_{INC} - (V_{GS} - V_{ON})$ characteristics as a function of trap depth, $E_C - E_T$ for a trap density of $N_T = 5 \times 10^{17}$ cm^{-3} and a drain voltage $V_{DS} = 0.2$ V. Model parameters used for this simulation: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu_{MODEL} = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

fills, the Fermi level is relatively remote from E_C such that there are few filled conduction band states; μ_{INC} is correspondingly small. However, once the trap is completely filled, the Fermi level abruptly rises toward E_C, resulting in an abrupt increase in the density of filled conduction band states and concomitantly in an abrupt increase in μ_{INC}. In contrast, for a shallow trap, the Fermi level is much closer to E_C such that conduction band filling and the μ_{INC} transition is less abrupt.

Figure 6.7 shows simulated μ_{AVG} and μ_{INC} curves as a function of trap density, N_T. μ_{AVG} is calculated at a drain voltage $V_{DS} = 0.1$ V and overvoltages of 1 V and 5 V, that is, $V_{GS} = V_{ON}+ 1$ V and $V_{GS} = V_{ON}+ 5$ V, respectively. μ_{INC} is calculated at $V_{GS} = 0.2$ V. Clearly above a certain trap density,

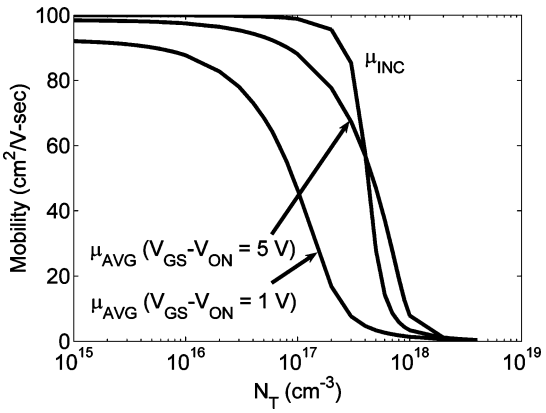

FIG. 6.7. Simulated μ_{INC} and μ_{AVG} characteristics as a function of trap density, N_T. Model parameters used for this simulation: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu_{MODEL} = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

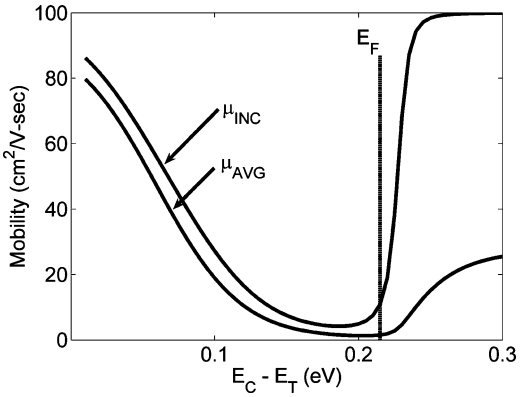

FIG. 6.8. Simulated μ_{INC} and μ_{AVG} characteristics as a function of trap depth, $E_C - E_T$. The Fermi level, E_F, as established by the initial free carrier concentration is 0.21 eV below the conduction band minimum, E_C. Model parameters used for this simulation: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu_{BULK} = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

$N_T \geq 3 \times 10^{17}$ cm^{-3} for this simulation, the mobility drastically decreases because most of the gate-induced channel electrons are trapped. On the other hand, when the trap concentration is reduced to less than $\sim 10^{17}$ cm^{-3}, μ_{INC} is not significantly affected by traps. At a small overvoltage, μ_{AVG} is more sensitive to the trap density, and never reaches the maximum bulk mobility even when the trap density is very low. At a large overvoltage and low trap density, μ_{AVG} approaches the bulk mobility, because the density of induced conduction band electrons is significantly larger than the trapped electron density.

Simulated μ_{AVG} and μ_{INC} curves as a function of trap depth, $E_C - E_T$, are shown in Figure 6.8. μ_{AVG} and μ_{INC} are calculated at a gate voltage of 1 V. The Fermi level, E_F, as established by the initial free carrier concentration, $n_{co} = 1 \times 10^{15}$ cm^{-3} is 0.21 eV below E_C. As $E_C - E_T$ increases, both μ_{AVG} and μ_{INC} monotonically decrease in a very similar manner until $E_T \sim E_F$. This trend is a consequence of the fact that a larger fraction of the gate voltage-induced electrons occupy trap states for a deeper trap. When E_T drops below E_F, both mobilities monotonically increase, and μ_{INC} attains a maximum value, μ_{MODEL}. When all the traps are deep and remain filled, they play no role in establishing μ_{INC} so that all of the electrons differentially induced into the channel by an incremental increase in the gate voltage occupy conduction band states. In contrast, μ_{AVG} is significantly smaller than μ_{INC} because it is a measure of all the electrons in the channel, the majority of which are trapped.

F. Unpatterned Channel, Fringing Current Artifacts

The width-to-length ratio, $\frac{Z}{L}$, is a key TFT parameter. For a TFT that has a clearly defined channel, $\frac{Z}{L}$ is given simply as the drawn width-to-length ratio. However, when a channel is unpatterned, peripheral current flows due to fringing electric fields outside the drawn channel. To correct for this peripheral current artifact, $\frac{Z}{L}$ must be replaced by an effective width-to-length ratio, $\frac{Z}{L}\big|_{EFF}$, as derived in the remainder of this section.

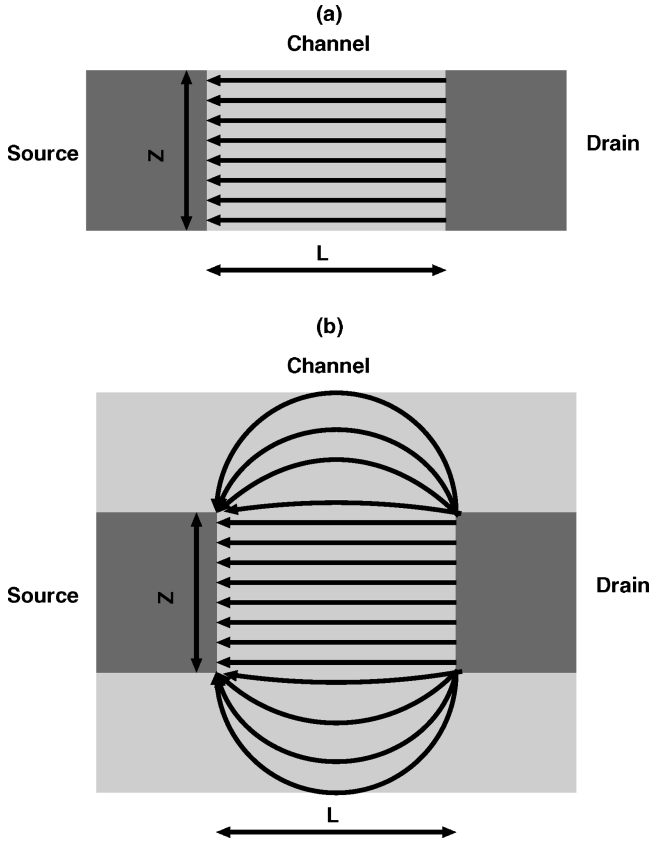

FIG. 6.9. Top-down views of two TFTs, showing the current pathways in (a) a TFT with a patterned channel and (b) a TFT with an unpatterned channel.

Figure 6.9 shows top-down views of two different TFTs with identical drawn widths (Z) and lengths (L) illustrating the current pathways in each device. In Figure 6.9(a), the channel is patterned. Thus, current (I_P) is restricted to the patterned region between the source and drain. In Figure 6.9(b), the channel is unpatterned. In this case, current is no longer restricted to the area between the source and drain. In addition to I_P, fringing current (I_F) also contributes to the total current. It is evident that the current in the TFT with an unpatterned channel is greater than in the TFT with a patterned channel. If this fringing current is not properly taken into account, an overestimated channel mobility is extracted from experimental data.

Returning to Figure 6.9, it can be seen that the current in the area between the source and drain is equivalent to I_P. Numerically this current is equal to[29]

$$I_P = \frac{Z}{L} G_{SH} V_{DS}, \qquad [6.12]$$

where G_{SH} is the sheet conductance and where it is assumed that V_{DS} is small enough that the TFT current flow can be modeled as resistive. There is also additional current, I_F, outside of the

area between the source and drain. An equation for I_F is derived assuming that the length of the source/drain contact is half the magnitude of Z. The current between such a configuration and, thus, the fringing current is given by[29]

$$I_F = \frac{\pi}{\ln 2} G_{SH} V_{DS}. \quad [6.13]$$

To find the total current in the unpatterned TFT, I_F and I_P are added together, yielding

$$I_D = I_F + I_P = \left(\frac{\pi}{\ln 2} + \frac{Z}{L}\right) G_{SH} V_{DS}. \quad [6.14]$$

Comparing the total current of an unpatterned device, Eq. 6.14, to the total current of a patterned device, Eq. 6.12, only the first terms differ. For the patterned device the first term is $\frac{Z}{L}$, whereas it is $(\frac{\pi}{\ln 2} + \frac{Z}{L})$ for the unpatterned device. Thus, an effective width-to-length ratio can be defined as

$$\left.\frac{Z}{L}\right|_{EFF} = \left(\frac{\pi}{\ln 2} + \frac{Z}{L}\right) \quad [6.15]$$

for an unpatterned device.

Returning to Eq. 6.14, notice that the first term, $(\frac{\pi}{\ln 2} + \frac{Z}{L})$, is a constant which depends on the TFT geometry, whereas the second term, $G_{SH}V_{DS}$, is a factor which depends on the current-voltage relationship used to model the TFT. Recognizing this, Eq. 6.14 can be generalized to

$$I_D = f(\textit{geometric parameters}) g(\textit{electrical parameters}), \quad [6.16]$$

where f and g denote functions involving the TFT geometry and the relevant current-voltage model, respectively. In Eq. 6.14, these functions are identified as

$$f(Z, L) = \left(\frac{\pi}{\ln 2} + \frac{Z}{L}\right), \quad [6.17]$$

assuming that the fringing current is modeled using a point-contact geometry, and

$$g(V_{GS}, V_{DS}) = G_{SH} V_{DS} \quad [6.18]$$

assuming that the TFT current flow is modeled as a resistor. If TFT current flow is modeled using square-law theory[2,19]

$$g(V_{GS}, V_{DS}) = \mu C_G \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right]. \quad [6.19]$$

where μ is mobility. For this situation, if the fringing current is modeled assuming a point-contact geometry,

$$I_P = \left(\frac{\pi}{\ln 2} + \frac{Z}{L}\right) g(V_{GS}, V_{DS}) \equiv \left.\frac{Z}{L}\right|_{EFF} g(V_{GS}, V_{DS}). \quad [6.20]$$

Thus, $\frac{Z}{L}|_{EFF}$, which constitutes a function of geometric parameters that includes fringing current in an unpatterned TFT, depends only on the device geometry, but not on how the TFT current-voltage characteristics are modeled.

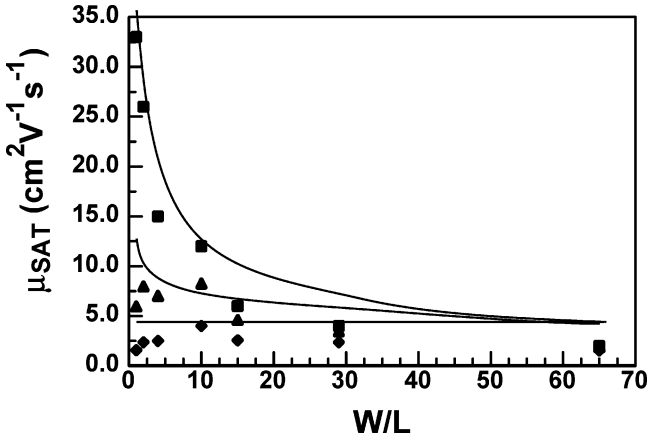

FIG. 6.10. Saturation mobility as a function of $\frac{Z}{L}$ for an unpatterned zinc oxide TFT. Three mobility trends are obtained using the drawn $\frac{Z}{L}$(squares), a point-contact model for fringing current (triangles), and an extracted equation for fringing current (diamonds). Because the term $\frac{\pi}{\ln 2}$ is equal to 4.53, the mobility can be significantly overestimated for TFTs with small $\frac{Z}{L}$ ratios.

For accurate mobility estimation of a nonpatterned TFT, $\frac{Z}{L}|_{EFF}$ should be used instead of $\frac{Z}{L}$ in mobility assessment equations such as Eqs. 6.7 or 6.8.

Mobility data obtained from the literature appears to confirm the existence of this fringing current artifact. Figure 6.10 shows the saturation mobility, μ_{SAT}, as a function of drawn $\frac{Z}{L}$ for an unpatterned zinc oxide TFT.[30] Saturation mobility is extracted from an $I_D - V_{GS}$ curve, measured with the device held in saturation and is calculated as[29]

$$\mu_{SAT} = \left.\frac{2m^2}{\frac{Z}{L} C_G}\right|_{Saturation}, \quad [6.21]$$

where m is the slope of a plot of I_{DSAT} against $(V_{GS} - V_T)$. Three mobility trends are included in Figure 6.10 and are obtained using drawn $\frac{Z}{L}$ (squares), $\frac{Z}{L}|_{EFF}$ assuming a half Z contact length geometry (triangles), and the following (diamonds)

$$\left.\frac{Z}{L}\right|_{EFF} = \left(20 + \frac{Z}{L}\right), \quad [6.22]$$

where Eq. 6.22 is deduced by changing the $\frac{\pi}{\ln 2}$ constant in Eq. 6.15 to obtain a flat mobility curve. The solid lines are guides for the eye, rather than least-square fits to the data. Notice that μ_{SAT} using the drawn $\frac{Z}{L}$ shows a dramatic increase as $\frac{Z}{L}$ decreases; this is unphysical. A more constant μ_{SAT} is seen by taking into account the fringing current point-contact model, although a slight curvature still exists, indicating that the point-contact model underestimates I_F. An almost flat mobility curve at ~2 cm^2/V-s is obtained using Eq. 6.22; this trend is more physically realistic and underscores the importance of using a patterned channel layer in a TFT in order to avoid fringing current artifacts, which can lead to an unrealistically large estimate of the channel mobility.

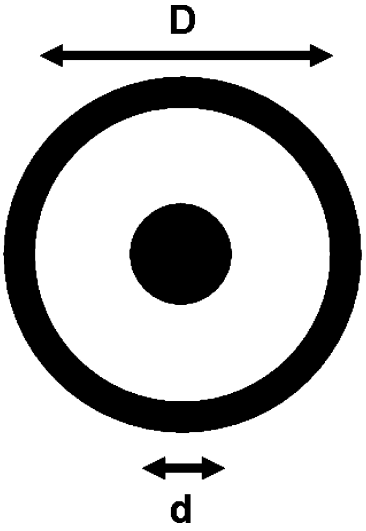

FIG. 6.11. Coaxial source-drain layout.

A more accurate assessment of mobility for a TFT with a blanket-coated, unpatterned channel layer is possible using the coaxial source-drain layout shown in Figure 6.11. In this configuration, current flows from the inner circle contact to the outer annulus contact, such that no fringing current artifact is possible. For the coaxial source-drain layout, the geometrical correction function is

$$f(d, D) = \left(\frac{2\pi}{\ln(D/d)}\right), \qquad [6.23]$$

where D is the inner diameter of the outer circle and d is the diameter of the inner circle of the annulus.

VII. CONCLUSIONS

The goal of this review article was to provide an overview of generic device physics–oriented TFT electrical modeling from the perspective of the development of new materials and emerging applications. Four models were considered: (i) square-law, (ii) 3-layer, (iii) comprehensive depletion-mode, and (iv) discrete trap. We hope that the models discussed herein will find use in the advancement of current, emerging, and future TFT technologies.

ACKNOWLEDGMENTS

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X. APPENDICES

A. Square-Law Model with Series Resistance

Building on the square-law model, resistors R_D and R_S are added at the source and the drain, as indicated in Figure 10.1. Internal voltages are calculated by applying Kirchhoff's current law to each node,

$$V'_D = V_{DS} - I_D R_D, \text{ and} \quad [10.1]$$

$$V'_S = I_D R_S. \quad [10.2]$$

Subtracting Eq. 10.1 from Eq. 10.2 results in the internal voltage across the TFT from drain to source,

$$V'_{DS} = V'_D - V'_S = V_{DS} - I_D (R_D + R_S). \quad [10.3]$$

Similarly, the internal voltage across the TFT from gate-to-source is found by applying Kirchhoff's voltage law,

$$V'_{GS} = V_{GS} - I_D R_S. \quad [10.4]$$

It should be noted that the non-primed quantities, V_{DS} and V_{GS}, represent the total external voltage applied across TFT terminals, whereas the primed quantities V'_{GS} and V'_{DS} are internal voltages across TFT terminals, thus accounting for the voltage dropped across R_S and R_D.

Equations 10.3 and 10.4 provide the necessary framework from which to begin an analysis of the effects of R_S and R_D on TFT performance. Inclusion of R_S and R_D into the equivalent circuit reduces the internal terminal voltages to V'_{GS} and V'_{DS}.

We conclude our analysis by rewriting the $I_D - V_{DS}$ equations for the pre- and post-pinch-off regimes in terms of the primed quantities V'_{GS} and V'_{DS}. Substituting Eqs. 10.3 and 10.4 into the square-law model equations, the resulting current-voltage equation for the pre-pinch-off regime is given by,

$$\begin{aligned} I_D &= \frac{ZC_G\mu}{L}\left(V'_{GS} - V_{ON} - \frac{V'_{DS}}{2}\right)V'_{DS} \\ &= \frac{ZC_G\mu}{L}\left(V_{GS} - I_D R_S - V_{ON} - \left(\frac{V_D - I_D(R_S + R_D)}{2}\right)\right) \\ &\quad \times (V_D - I_D(R_S + R_D)) \end{aligned} \quad [10.5]$$

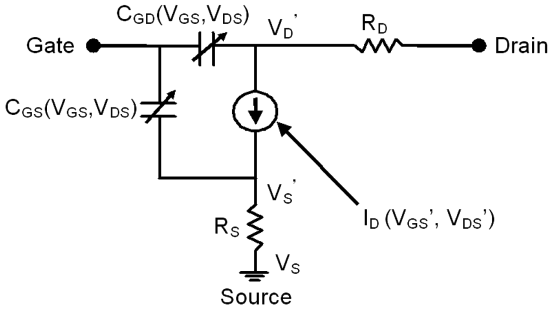

FIG. 10.1. Square-law model equivalent circuit for a TFT that includes the effects of source and drain series resistance. Primed quantities represent internal voltages.

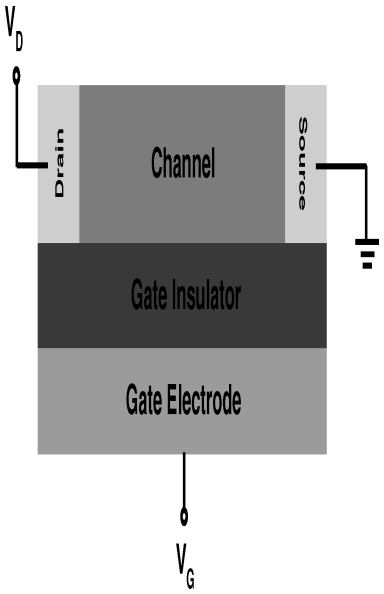

FIG. 10.2. Simplified cross-section diagram of a thin-film transistor.

whereas the corresponding equation for the post-pinch-off regime becomes,

$$\begin{aligned} I_D &= \frac{ZC_G\mu}{2L}(V'_{GS} - V_{ON})^2 \\ &= \frac{ZC_G\mu}{2L}(V_{GS} - I_D R_S - V_{ON})^2 \end{aligned} \quad [10.6]$$

Finally, demarcation between the pre- and the post-pinch-off regime is established by the pinch-off voltage, which for this square-law with series resistance model is given by,

$$V_{DSAT} = V_{GS} - V_{ON} + I_D R_D. \quad [10.7]$$

B. Conductance Integral Equation Modeling

1. Conductance Integral Equation

Figure 10.2 shows a simple bottom-gate TFT. Source and drain contacts are idealized so that the cross-section of the channel is uniform from source to drain. The biasing scheme is as follows: the source is grounded, V_G is applied to the gate, and V_D is applied to the drain. Voltage in the channel, V_C, varies from 0 V at the source to V_D at the drain. Conductivity of the channel varies from the source to the drain and depends on both V_G and V_C.

Hoffman derives a general field-effect transistor equation relating current to voltage for an n-channel device as[31]

$$I = \frac{Z}{L}\int_0^{V_{DS}} G(V_C)dV, \quad [10.8]$$

where G is the conductance of the channel as a function of voltage along the channel.

In order to proceed further, we define V_{CH} as,

$$V_{CH} = V_{GS} - V(y). \quad [10.9]$$

V_{CH} is the portion of the applied gate voltage that acts to induce or deplete charge at a given location along the channel. With the change of variable $V \rightarrow V_{CH}$, Eq. 10.8 becomes

$$I_D = \int_{V_{GD}}^{V_{GS}} G(V_{CH}) dV_{CH}. \qquad [10.10]$$

where V_{GD} is the gate voltage measured with respect to the drain and is equal to $V_{GS} - V_{DS}$.

Now, consider $G(V_{CH})$. This term is the conductance of the channel with respect to V_{CH}. The function relating G to V_{CH} can be found by analyzing the transistor in the linear regime of TFT operation. The linear regime occurs when $V_{DS} \sim 0$ V. In the linear regime of operation, the channel conductivity is approximately uniform across the channel, in accordance with the gradual channel approximation. Therefore, the conductance can be expressed as

$$G(V_{CH}) = \frac{G_D^{LIN}(V_{CH})}{\frac{Z}{L}}, \qquad [10.11]$$

where G_D^{LIN} explicitly specifies that the channel conductance is evaluated in the linear regime of operation. Also recognize that in the linear regime of operation, the source is at ground potential and the drain is very close to ground potential; thus, the entire channel is essentially grounded. Therefore, V_{CH} is approximately equal to the applied gate voltage V_G. This being the case, Eq. 10.11 may be approximated as

$$G(V_{CH}) \approx \frac{G_D^{LIN}(V_G)}{\frac{Z}{L}}. \qquad [10.12]$$

Substituting Eq. 10.12 into Eq. 10.10 yields

$$I_D = \int_{V_{GD}}^{V_{GS}} G_D^{LIN}(V_G) dV_G. \qquad [10.13]$$

Equation (10.13), the conductance integral equation, asserts that I_D can be calculated for all V_{DS} and V_{GS} values if the drain conductance evaluated in the linear regime is known over a sufficiently wide range of V_G. I_D at any V_{GS} and V_{DS} is simply the area under a $G_D^{LIN} - V_G$ curve from V_{GD} to V_{GS}, as shown in section X.B.2. In terms of measured quantities, G_D^{LIN} is calculated as

$$G_D^{LIN} = \left. \frac{I_D(V_{GS}, V_{DS})}{V_{DS}} \right|_{V_{DS} \rightarrow 0}. \qquad [10.14]$$

An important modeling consequence of the conductance integral equation is that different functional forms of $G_D^{LIN}(V_G)$ give rise to different mathematical forms of $I_D(V_{GS}, V_{DS})$, which can be utilized to model the effects of mobility variation with applied gate voltage.[31]

A significant implication of the conductance integral equation is that $G_D^{LIN} - V_{GS}$ can be calculated from a single $I_D - V_{DS}$ curve. Rearrangement of Eq. 10.14 results in[24]

$$G_D^{LIN}(V_{GS} - V_{DS}) = \frac{dI_D(V_{GS}, V_{DS})}{dV_{DS}}. \qquad [10.15]$$

Equation 10.15 states that the slope of an $I_D - V_{DS}$ curve evaluated at V_{DS} and V_{GS} yields G_D^{LIN} evaluated at $V_{GS} - V_{DS}$. This is illustrated in Figure 10.3. The top curve shown in Figure 10.3(a) corresponds to $V_{GS} = 40$ V. The slope of this I_D-V_{DS} curve at $V_{DS} = 10$ V, as indicated by the arrow, is equal to G_D^{LIN} assessed at a value of $V_{GS} - V_{DS} = 40$ V $- 10$ V $= 30$ V, as indicated in Figure 10.3(b) by the solid circle. This method for extracting $G_D^{LIN}(V_G)$ can aid in channel mobility estimation in situations in which accurate G_D^{LIN} assessment is not possible because the linear regime of operation for an $I_D - V_{DS}$ curve is dominated by a barrier contact or gate leakage.

2. *Enhancement-Mode Current Model*

In this section, the conductance integral equation, Eq. 10.13, is used to derive an $I_D(V_{GS}, V_{DS})$ equation for an enhancement-mode TFT. The equation derived is then shown to be equivalent to the square-law model for a TFT.[2,19] Figure 10.4 shows a

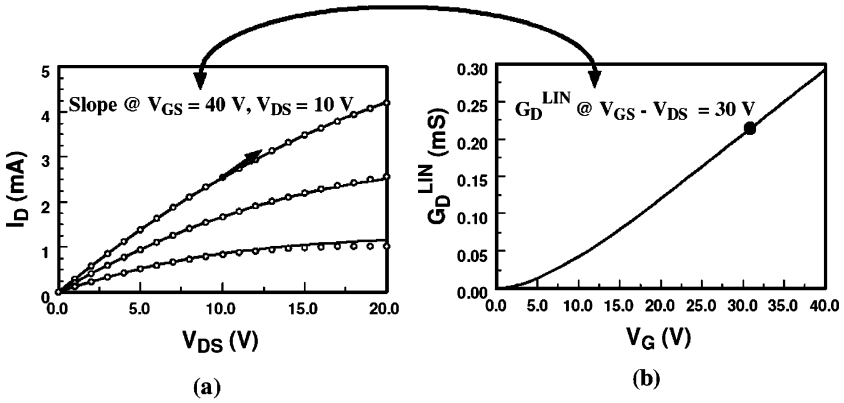

FIG. 10.3. (a) I_D-V_{DS} and (b) G_D^{LIN}-V_G characteristics of a zinc tin oxide TFT. The solid lines shown in (a) are calculated curves from measured G_D^{LIN} data shown in (b), using the conductance integral equation. The circles shown in (a) are measured data. V_{GS} is decreased from 40 V (top curve, showing maximum current) to 20 V in 10 V steps. The arrow shown in (a) indicates the slope of the I_D-V_{DS} line at $V_{GS} = 40$ V, $V_{DS} = 10$ V which is equal to G_D^{LIN} at $V_G = 30$ V, as indicated by the solid circle shown in (b).

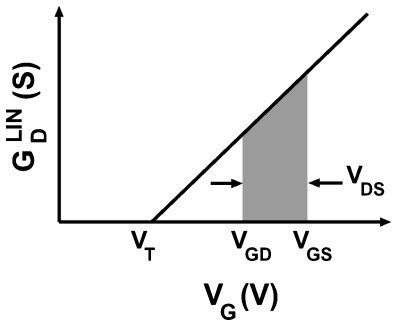

FIG. 10.4. $G_D^{LIN} - V_G$ plot for an idealized transistor. The equation of this line is $\frac{Z\mu C_G}{L}(V_G - V_T)$. V_{DS} corresponds to the difference between V_{GS} and V_{GD}. The area of the shaded region under the G_D^{LIN} curve evaluated between V_{GS} and V_{GD} corresponds to I_D.

$G_D^{LIN} - V_G$ characteristic for an idealized transistor, in which the channel conductance in the linear region is modeled as[32]

$$G_D^{LIN} = \frac{Z\mu C_G}{L}(V_G - V_T), \qquad [10.16]$$

where μ is the carrier mobility (assumed to be constant with respect to V_{GS}) and V_T is the threshold voltage. V_{GS} is the applied voltage from the gate to the source. V_{GD} is the applied voltage from the gate to the drain. V_{DS} is the difference between V_{GD} and V_{GS}. The shaded region corresponds to I_D, as described by Eq. [10.13].

Now consider the mathematical consequence of Figure 10.4 in conjunction with the conductance integral equation. Substituting Eq. 10.16 into Eq. 10.13,

$$\begin{aligned} I_D &= \int_{V_{GD}}^{V_{GS}} \frac{Z\mu C_G}{L}(V_G - V_T)dV_G \\ &= \frac{Z\mu C_G}{L}\left[\frac{V_{GS}^2}{2} - V_{GS}V_T - \frac{V_{GD}^2}{2} - V_{GD}V_T\right]. \end{aligned} \qquad [10.17]$$

Notice from Figure 10.4 that

$$V_{GD} = V_{GS} - V_{DS}. \qquad [10.18]$$

Substituting Eq. 10.18 into Eq. 10.17 and collecting terms yields

$$I_D = \frac{Z\mu C_G}{L}\left[(V_{GS} - V_T)\,V_{DS} - \frac{V_{DS}^2}{2}\right]. \qquad [10.19]$$

This equation is valid for V_{GD} greater than V_T. Returning to Figure 10.4, notice that for values of V_G less than V_T, G_D^{LIN} is zero and there is no area under the $G_D^{LIN} - V_G$ curve. If V_{GS} is held constant, the maximum area of the shaded region is reached when $V_{GD} = V_T$. At this point, the channel is pinched off and saturation occurs so that

$$I_D \equiv I_{DSAT} = \frac{Z\mu C_G}{2L}(V_{GS} - V_T)^2. \qquad [10.20]$$

As V_{GD} is reduced below V_T, or if the gate is held constant as V_{DS} is increased above $V_{GS} - V_T$, the area of the shaded region, I_D, does not increase. I_D saturates at this point. Decreasing V_{GD} below V_T (i.e., increasing V_{DS} above $V_{GS} - V_T$) has no effect on I_D.

Note that Eqs. 10.19 and 10.20 correspond to the square-law model pre- and post-pinch-off current-voltage characteristics for an ideal long-channel transistor.[2,19] As shown earlier, the square-law model is derived from the conductance integral equation assuming that channel conductance in the linear region is directly proportional to the gate voltage.

3. *Comprehensive Depletion-Mode Current Model*

In this section, the current-voltage characteristics are derived for a depletion-mode TFT. First, expressions for $G_D^{LIN}(V_G)$ are developed. Then, these expressions for $G_D^{LIN}(V_G)$ are substituted into the conductance integral equation in order to generate a corresponding set of current-voltage relationships.

a. Depletion-mode conductance. Consider an n-channel TFT with a channel carrier concentration N_D. Application of a positive bias to the gate induces an electron accumulation region in the channel. In contrast, application of a negative bias results in depletion of the channel. Because appreciable drain current can flow in a depletion-mode TFT in both depletion and accumulation, the channel conductance must be modeled in both regimes of operation.

For a depletion-mode TFT, the linear regime channel conductance, $G_D^{LIN}(V_G)$, is modeled as[32]

$$G_D^{LIN} = \frac{Z}{L}\mu q N_e, \qquad [10.21]$$

where N_e is the number of mobile electrons per cm^2 of gate area. In accumulation, the electron density in the channel is comprised of bulk electrons already present due to doping and of electrons which are induced in the channel as a consequence of the application of a gate voltage,[32]

$$N_e = N_D h + V_G C_G, \qquad [10.22]$$

where h is the channel thickness. Thus, for a depletion-mode TFT operating in accumulation

$$G_D^{LIN}|_{ACC} = \frac{Z}{L}\mu q(N_D h + V_G C_G). \qquad [10.23]$$

In depletion, the electron density in the channel decreases as the gate voltage-induced depletion region widens,

$$N_e = N_D\,(h - W_{DEP}), \qquad [10.24]$$

where W_{DEP} is the depletion space charge width. W_{DEP} is given by[33]

$$W_{DEP} = \left(\frac{\varepsilon_S^2}{C_G^2} - \frac{2V_G\varepsilon_S}{qN_D}\right)^{\frac{1}{2}} - \frac{\varepsilon_S}{C_G}, \qquad [10.25]$$

where ε_S is the permittivity of the channel. Here we define two new terms, $C_S = \frac{\varepsilon_S}{h}$, corresponding to the semiconductor (i.e., the channel) capacitance, and the pinch-off voltage, V_P, which

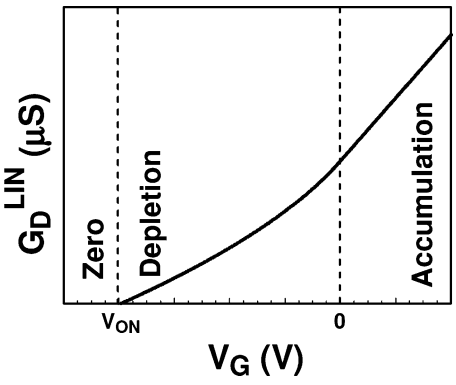

FIG. 10.5. $G_D^{LIN} - V_G$ plot for an idealized depletion-mode TFT.

corresponds to the gate voltage required to completely deplete the channel if no insulator is present and is calculated as[32]

$$V_P = -\frac{qN_D h^2}{2\varepsilon_S}. \quad [10.26]$$

Substituting C_S and V_P into Eq. 10.25 and factoring out h, yields

$$W_{DEP} = h\left[\left(\frac{C_S^2}{C_G^2} + \frac{V_G}{V_P}\right)^{\frac{1}{2}} - \frac{C_S}{C_G}\right]. \quad [10.27]$$

Substituting Eq. 10.27 into Eq. 10.24 yields

$$N_e = N_D\left[1 + \frac{C_S}{C_G} - \left(\frac{C_S^2}{C_G^2} + \frac{V_G}{V_P}\right)^{\frac{1}{2}}\right]. \quad [10.28]$$

Finally, substituting Eq. 10.28 into Eq. 10.21 yields the G_D^{LIN} relation appropriate for a depletion-mode TFT operating in depletion

$$G_D^{LIN}\big|_{DEPL} = \frac{Z}{L}\sigma\left[1 + \frac{C_S}{C_G} - \left(\frac{C_S^2}{C_G^2} + \frac{V_G}{V_P}\right)^{\frac{1}{2}}\right], \quad [10.29]$$

where σ is the conductivity of the channel and is calculated as

$$\sigma = \mu q N_D. \quad [10.30]$$

Equations 10.23 and 10.29 constitute the G_D^{LIN} relations required to generate the current-voltage characteristic equations appropriate for a depletion-mode TFT.

b. Depletion-mode current voltage characteristics.. Figure 10.5 shows the $G_D^{LIN} - V_G$ characteristics of an idealized n-channel depletion-mode TFT. Three regions of conductance are shown; the zero region, where the conductance is zero, the depletion region, and the accumulation region, where G_D^{LIN} is evaluated via Eqs. 10.29 and 10.23, respectively.

Figure 10.6 shows the cross-section and corresponding $G_D^{LIN} - V_G$ plots of three operating regions for an n-channel, depletion-mode TFT. Figure 10.6(a) shows the device with applied voltages such that a depletion region exists in the channel from the source to drain. Figure 10.6(b) shows the device with applied voltages such that an accumulation region exists in the channel from the source to the drain. Figure 10.6(c) shows the intermediate case in which the channel is partially depleted and partially accumulated.

First, consider the depleted channel case indicated in Figure 10.6(a). A depletion region exists in the channel from the source to the drain, when both V_{GD} and V_{GS} are between V_{ON} and zero volts. In this region of operation, the conductance through the entire channel is modeled using Eq. 10.29. Substituting Eq. 10.29 into the conductance integral equation, Eq. 10.13, yields the drain current as,

$$I_D = \frac{Z}{L}\sigma h\left[\left(1 + \frac{C_S}{C_G}\right)V_{DS} - \frac{2}{3}V_P\left(\left(\frac{C_S^2}{C_G^2} + \frac{V_{GS}}{V_P}\right)^{\frac{3}{2}} - \left(\frac{C_S^2}{C_G^2} + \frac{V_{GD}}{V_P}\right)^{\frac{3}{2}}\right)\right], \quad [10.31]$$

which is valid in the pre-pinchoff region of operation. If V_{GS} is held constant, the maximum drain current is reached when $V_{GD} = V_{ON}$. At this point, the channel is pinched off and saturation occurs so that

$$I_D = \frac{Z}{L}\sigma h\left[\left(1 + \frac{C_S}{C_G}\right)V_{DSAT} - \frac{2}{3}V_P\left(\left(\frac{C_S^2}{C_G^2} + \frac{V_{GS}}{V_P}\right)^{\frac{3}{2}} - \left(\frac{C_S^2}{C_G^2} + \frac{V_{ON}}{V_P}\right)^{\frac{3}{2}}\right)\right], \quad [10.32]$$

where

$$V_{DS}(V_{GD} = V_{ON}) \equiv V_{DSAT} = V_{GS} - V_{ON}. \quad [10.33]$$

As V_{GD} is reduced below V_{ON}, or if the gate is held constant as V_{DS} is increased above V_{DSAT}, I_D does not increase. Equations 10.32 and 10.33 constitute current-voltage characteristics describing an n-channel, depletion-mode TFT operating in channel depletion for the pre-pinch-off and post-pinch-off regions, respectively.

Next, consider the accumulated-channel case shown in Figure 10.6(b). The channel near the source is accumulated when $V_{GS} > 0$ V and the channel near the drain is accumulated when $V_{GD} > 0$ V. Because accumulation occurs throughout the entire length of channel, G_D^{LIN} is calculated using Eq. 10.23. Substituting Eq. 10.23 into the conductance integral equation (Eq. 10.13) yields the drain current as,

$$I_D = \frac{Z}{L}\left[\mu C_G\left(V_{GS}V_{DS} - \frac{V_{DS}^2}{2}\right) + \sigma h V_{DS}\right]. \quad [10.34]$$

Equation 10.35 is the pre-pinch-off current-voltage relationship describing an n-channel, depletion-mode TFT operating in accumulation along the entire channel length. Note that this equation corresponds to the pre-pinch-off square-law model in parallel with a resistor. The pre-pinch-off square-law portion represents the accumulation channel current, whereas the parallel resistor represents current through the bulk channel. Note that this expression is equivalent to the 3-layer model of section IV.A, if the surface accumulation layer is ignored.

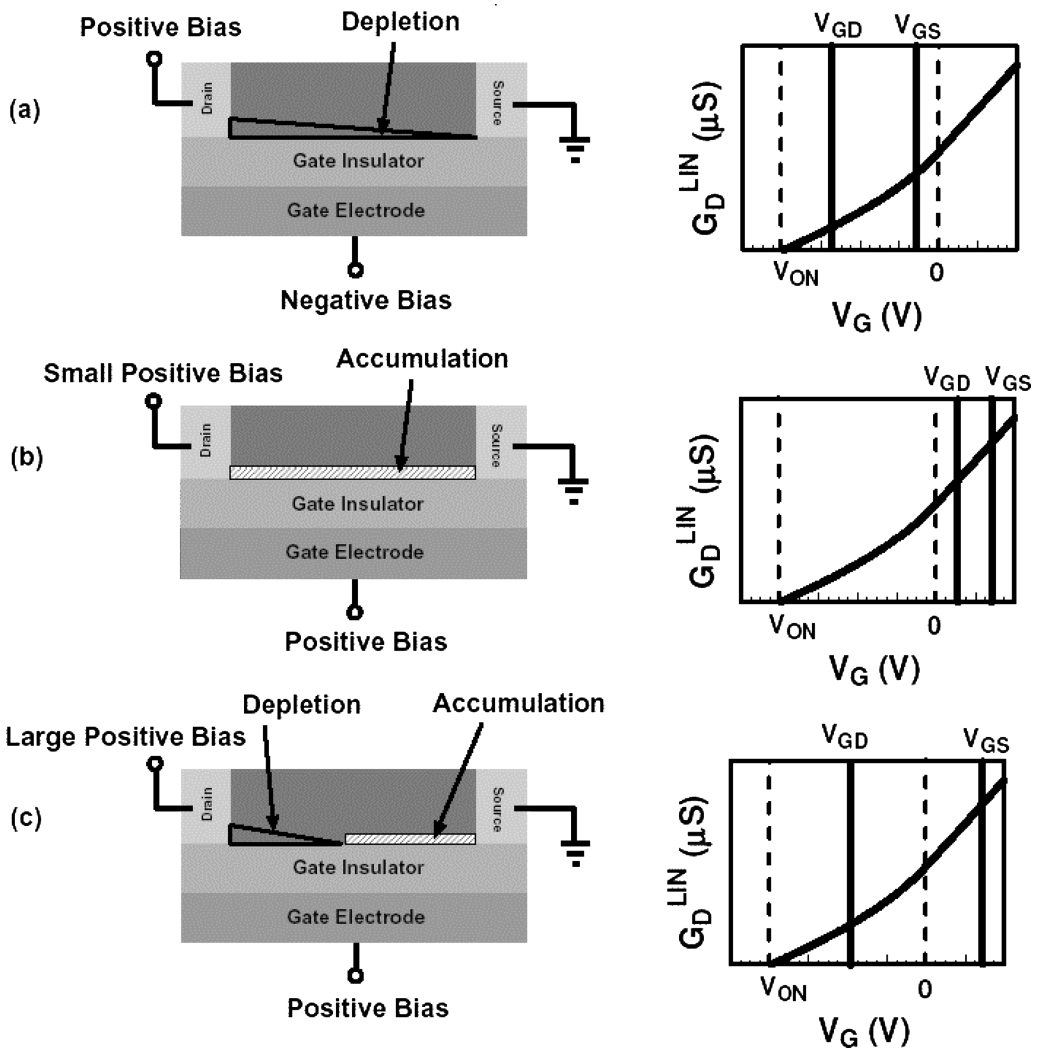

FIG. 10.6. Depletion-mode TFT cross-section and corresponding $G_D^{LIN} - V_G$ plot showing three operating conditions: (a) the channel has a depletion region extending from the source to the drain, (b) the channel has an accumulation region extending from the source to the drain, and (c) the channel is depleted near the drain and is accumulated near the source. Note that the magnitude of V_{GD} and V_{GS} with respect to V_{ON} and zero volts determine which operating region applies.

If the drain voltage is increased, such that V_{GD} decreases below 0 V, the channel near the drain is fully depleted, resulting in the situation shown in Figure 10.6(c). Because both an accumulation region and a depletion region exist along the length of the channel, both Eq. 10.23 and Eq. 10.29 must be used to calculate the channel conductance. Substituting both of these into the conductance integral equation, Eq. 10.13, yields

$$I_D = \int_{V_{GD}}^{0} G_D^{LIN}(V_G)\big|_{ACC} dV_G + \int_{0}^{V_{GS}} G_D^{LIN}(V_G)\big|_{DEPL} dV_G. \quad [10.35]$$

Notice that this results in two integrals, one integral evaluating G_D^{LIN} for the accumulation region and one integral evaluating G_D^{LIN} for the depletion region. Evaluating these integrals leads to

$$I_D = I_{ACC} + I_{DEPL}, \quad [10.36]$$

where

$$I_{ACC} = \frac{Z\mu C_G}{2L} V_{GS}^2 + \frac{Zh\sigma}{L} V_{GS}, \quad [10.37]$$

and

$$I_{DEPL} = \frac{Z}{L}\sigma h\left[\left(1 + \frac{C_S}{C_G}\right)(V_{DS} - V_{GS}) - \frac{2}{3}V_P\left(\frac{C_S^3}{C_G^3} - \left(\frac{C_S^2}{C_G^2} + \frac{V_{GD}}{V_P}\right)^{\frac{3}{2}}\right)\right]. \quad [10.38]$$

Decreasing V_{GD} below V_{ON} again leads to a saturated I_D which

is calculated as

$$I_D = I_{ACC} + I_{DEPL2}, \quad [10.39]$$

where

$$I_{DEPL2} = \frac{Z}{L}\sigma h\left[\left(1+\frac{C_S}{C_G}\right)(V_{ON}) - \frac{2}{3}V_P\left(\frac{C_S^3}{C_G^3} - \left(\frac{C_S^2}{C_G^2}+\frac{V_{ON}}{V_P}\right)^{\frac{3}{2}}\right)\right]. \quad [10.40]$$

Equations 10.37 and 10.40 constitute the pre-pinch-off and post-pinch-off current-voltage characteristics describing an n-channel, depletion-mode TFT operating in a partially depleted and partially accumulated channel, as illustrated in Figure 10.6(c).

C. Discrete Trap Model Derivation

The discrete trap under consideration is assumed to be characterized by its ionization energy, E_T, capture cross-section, σ_n, and density, N_t.

If the density of filled traps is given by n_t, the rate of conduction band trapping is given by $\bar{v}\sigma_n(N_t - n_t)n_c$, where $\bar{v}$ is the average conduction band electron velocity, $(N_t - n_t)$ is the density of empty traps, and n_c is the density of electrons present in the conduction band. Also, the rate of electron emission from this trap state to the conduction band is given by $\bar{v}\sigma_n n_t n_1$, where n_1 is the conduction band electron density when the Fermi-level is equal to the trap level. n_1 is given by

$$n_1 = N_c e^{\left(\frac{-E_T}{k_B T}\right)}, \quad [10.41]$$

where N_c is the effective density of states of the conduction band and k_B is Boltzmann's constant. Thus, the net rate of change in trap occupancy is given by

$$\frac{\partial n_t}{\partial t} = \overline{v}\sigma_n(N_t - n_t)n_c - \bar{v}\sigma_n n_t n_1. \quad [10.42]$$

In steady-state, the rate of trap emission and capture are equal so that

$$(N_t - n_t)n_c = n_t n_1. \quad [10.43]$$

Solving for n_t yields an explicit assessment of the steady-state trap occupancy,

$$n_t = \frac{n_c N_t}{n_c + n_1}. \quad [10.44]$$

Recognizing that the total charge induced in the channel by the application of a gate voltage is distributed into both conduction band and trap states,

$$q(\Delta n_c + \Delta n_t) = q[(n_c + n_t) - (n_{co} + n_{to})] = \frac{C_G}{h}[V_{GS} - V(y)], \quad [10.45]$$

where n_{co} and n_{to} are the initial, zero-bias densities of free conduction band electrons and trapped electrons. Rearrangement of Eq. 10.46 leads to

$$q(n_c + n_t) = \frac{C_G}{h}[V_{GS} - V(y) - V_{ON}], \quad [10.46]$$

where $V_{ON} = -\frac{qh}{C_G}(n_{co} + n_{to})$.

Substitution of n_t from Eq. 10.45 into Eq. 10.47 yields,

$$V_c(y) \equiv \frac{qn_c(y)h}{C_G} = \frac{1}{2}[(V_{GS} - V(y) - V_{ON}) - (V_t + V_1)] + \frac{1}{2}\{[(V_{GS} - V(y) - V_{ON}) - (V_t + V_1)]^2 + 4V_1(V_{GS} - V(y) - V_{ON})\}^{1/2}, \quad [10.47]$$

where $V_t = \frac{qN_t h}{C_G}$ and $V_1 = \frac{qn_1 h}{C_G}$.

For mathematical convenience, Eq. 10.49 can be rewritten as

$$V_c(y) = \frac{1}{2}[a - V(y)] + \frac{1}{2}\{[a - V(y)]^2 + c[b - V(y)]\}^{1/2}, \quad [10.48]$$

where, $a = V_{GS} - V_t - V_{ON} - V_1$, $b = V_{GS} - V_{ON}$ and $c = 4V_1$.

Drift-dominated drain current is derived in a similar manner as the ideal square-law derivation,[19] beginning with

$$I_D = hZn_c(y)q\mu\frac{dV(y)}{dy}. \quad [10.49]$$

Substitution of $n_c(y)$ from Eq. 10.49 into Eq. 10.51, operating on both sides by dy, integrating the left hand side of the equation over the channel length and dividing both sides of the equation by L leads to,

$$I_D = \frac{Z}{L}\mu C_G\int_0^{V_{DS}} V_c(y)dV(y). \quad [10.50]$$

Substitution of Eq. 10.50 for $V_c(y)$ into Eq. 10.52 and performing the integration yields,

$$I_D = \frac{Z}{L}\mu C_G\left[\frac{1}{2}aV_{DS} - \frac{1}{4}V_{DS}^2 + \frac{1}{4}\left(V_{DS} - a - \frac{c}{2}\right)C_1 + \ln\left(\frac{C_2}{C_3}\right)(V_t V_1) + \frac{1}{4}(a^2 + bc)^{1/2}\left(a + \frac{c}{2}\right)\right], \quad [10.51]$$

where, $C_1 = [(a - V_{DS})^2 + c(b - V_{DS})]^{1/2}$, $C_2 = (-2a - c + 2V_{DS} + 2C_1)$, and $C_3 = [-2a - c + 2(a^2 + bc)^{1/2}]$. Equation 10.53 constitutes the discrete trap model current-voltage characteristic equation for the pre-pinch-off regime of the TFT operation, whose independent variable constraint equation are specified by

$$V_{GS} \geq V_{ON} \quad \text{and} V_{DS} \leq V_{DSAT}. \quad [10.52]$$

The drain current expression for the saturation (post-pinch-off) regime of TFT operation is then obtained by replacing V_{DS} by

V_{DSAT} in Eq. 10.53 and requiring that $V_{DS} \geq V_{DSAT}$. Explicitly the post-pinch-off current-voltage expression is given by

$$I_{DSAT} = \frac{Z}{L}\mu C_G\left[\frac{1}{2}aV_{DSAT} - \frac{1}{4}V_{DSAT}^2 + \frac{1}{4}\left(V_t^2 - V_1^2\right) + \ln\left(\frac{4V_t}{C_3}\right)(V_t V_1) + \frac{1}{4}(a^2+bc)^{1/2}\left(a+\frac{c}{2}\right)\right], \quad [10.53]$$

where the corresponding constraint equations are given by

$$V_{GS} \geq V_{ON} \quad \text{and } V_{DS} > V_{DSAT}. \quad [10.54]$$

Finally, the pinch-off voltage for the discrete trap model is given by

$$V_{DSAT} = V_{GS} - V_{ON}. \quad [10.55]$$